

# Intel® Desktop Board D946GZIS Technical Product Specification

*September 2006*

*Order Number: D56025-002US*

The Intel® Desktop Board D946GZIS may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D946GZIS Specification Update.

# Revision History

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Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D946GZIS Technical Product Specification.	July 2006
-002	Second release of the Intel® Desktop Board D946GZIS Technical Product Specification. Removed references to DDR2 800 memory support.	September 2006

This product specification applies to only the standard Intel® Desktop Board D946GZIS with BIOS identifier TS94610J.86A.

Changes to this specification will be published in the Intel Desktop Board D946GZIS Specification Update before being incorporated into a revision of this document.

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# Preface

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This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board D946GZIS. It describes the standard product and available manufacturing options.

## Intended Audience

The TPS is intended to provide detailed, technical information about the Desktop Board D946GZIS and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

## What This Document Contains

Chapter	Description
1	A description of the hardware used on the board
2	A map of the resources of the board
3	The features supported by the BIOS Setup program
4	A description of the BIOS error messages, beep codes, and POST codes

## Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

## Notes, Cautions, and Warnings

### **NOTE**

*Notes call attention to important information.*

### **INTEGRATOR'S NOTES**

*Integrator's notes are used to call attention to information that may be useful to system integrators.*

### **CAUTION**

*Cautions are included to help you avoid damaging hardware or losing data.*

## Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
GB	Gigabyte (1,073,741,824 bytes)
GB/sec	Gigabytes per second
Gbit	Gigabit (1,073,741,824 bits)
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbit/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

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# 1 Product Description

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## 1.1 Overview

### 1.1.1 Feature Summary

Table 1 summarizes the major features of the Desktop Board D946GZIS.

**Table 1. Feature Summary**

<b>Form Factor</b>	microATX (9.60 inches by 9.60 inches [243.84 millimeters by 243.84 millimeters])
<b>Processor</b>	Support for the following: <ul style="list-style-type: none"> <li>• Intel® Core™2 Duo processor in an LGA775 socket with a 1066 or 800 MHz system bus</li> <li>• Intel® Pentium® D processor in an LGA775 socket with an 800 or 533 MHz system bus</li> <li>• Intel® Pentium® 4 processor in an LGA775 socket with an 800 or 533 MHz system bus</li> <li>• Intel® Celeron® D processor in an LGA775 socket with a 533 MHz system bus</li> </ul>
<b>Memory</b>	<ul style="list-style-type: none"> <li>• Two 240-pin DDR2 SDRAM Dual Inline Memory Module (DIMM) sockets</li> <li>• Support for DDR2 667 or DDR2 533 MHz DIMMs</li> <li>• Support for up to 4 GB of system memory</li> </ul>
<b>Chipset</b>	Intel® 946GZ Express Chipset, consisting of: <ul style="list-style-type: none"> <li>• Intel® 82946GZ Graphics and Memory Controller Hub (GMCH)</li> <li>• Intel® 82801GB I/O Controller Hub (ICH7)</li> </ul>
<b>Video</b>	Intel® GMA 3000 onboard graphics subsystem
<b>Audio</b>	6-channel (5.1) audio subsystem using the ADI1988A (or SigmaTel* STAC9227) audio codec
<b>Legacy I/O Control</b>	Legacy I/O controller for diskette drive, serial, parallel, and PS/2* ports
<b>USB</b>	Support for USB 2.0 devices
<b>Peripheral Interfaces</b>	<ul style="list-style-type: none"> <li>• Eight USB ports</li> <li>• Four Serial ATA IDE interfaces</li> <li>• One Parallel ATA IDE interface with UDMA 33, ATA-66/100 support</li> <li>• One diskette drive interface</li> <li>• One serial port</li> <li>• One parallel port</li> </ul>
<b>LAN Support</b>	10/100 Mbps/sec LAN subsystem using the Intel® 82562G Platform LAN Connect (PLC) device
<b>BIOS</b>	<ul style="list-style-type: none"> <li>• Intel® BIOS (resident in the SPI Flash device)</li> <li>• Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS</li> </ul>
<b>Instantly Available PC Technology</b>	<ul style="list-style-type: none"> <li>• Support for PCI Local Bus Specification Revision 2.3</li> <li>• Support for PCI Express* Revision 1.0a</li> <li>• Suspend to RAM support</li> <li>• Wake on PCI, RS-232, front panel, PS/2 devices, and USB ports</li> </ul>

continued

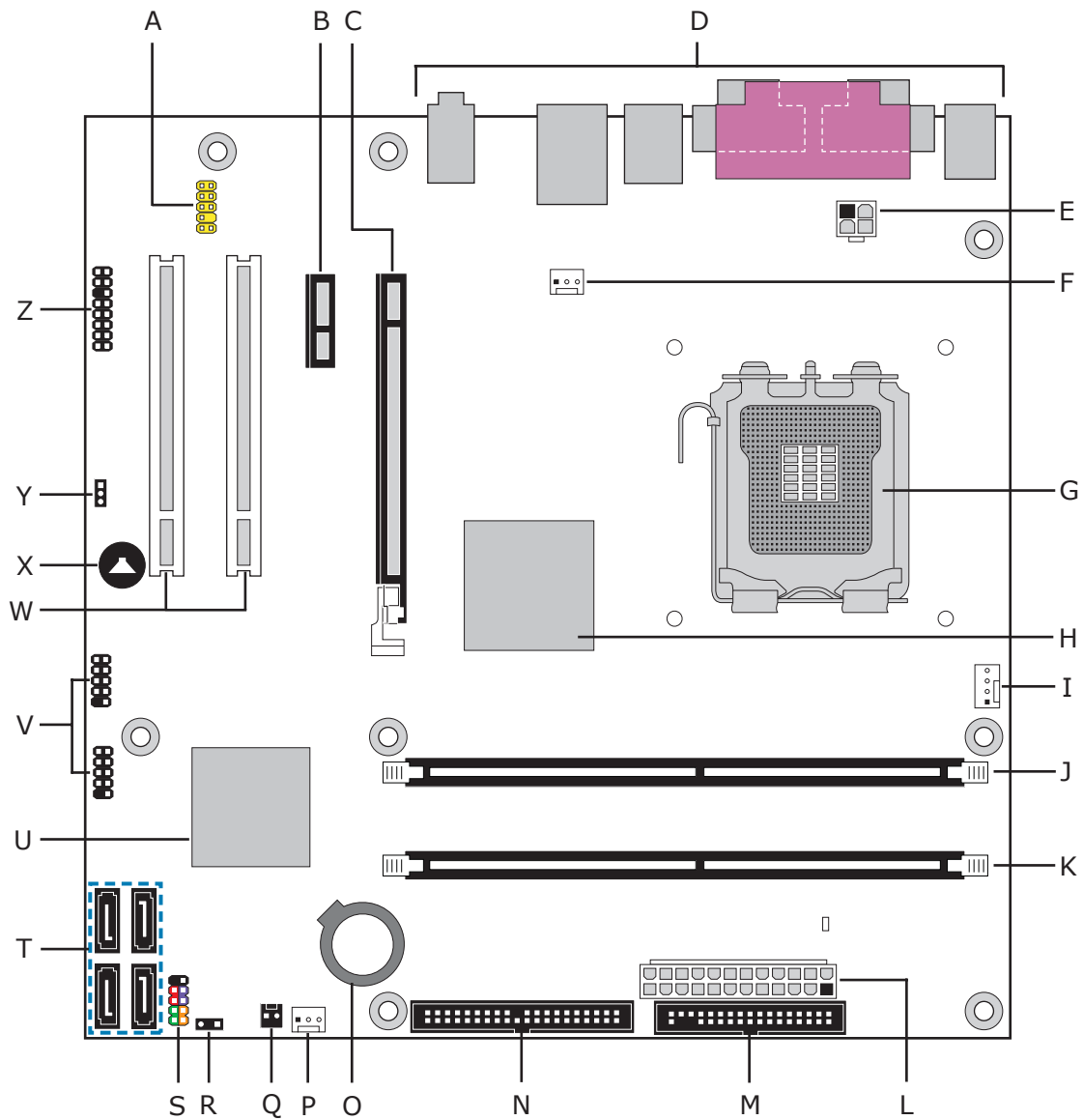
**Table 1. Feature Summary (continued)**

<b>Expansion Capabilities</b>	<ul style="list-style-type: none"> <li>• One PCI Express x16 bus add-in card connector</li> <li>• One PCI Express x1 bus add-in card connector</li> <li>• Two PCI Conventional* bus connectors</li> </ul>
<b>Hardware Monitor Subsystem</b>	<ul style="list-style-type: none"> <li>• Voltage sense to detect out of range power supply voltages</li> <li>• Thermal sense to detect out of range thermal values</li> <li>• Three fan headers</li> <li>• Three fan sense inputs used to monitor fan activity</li> </ul>

<b>For information about</b>	<b>Refer to</b>
Available configurations for the Desktop Board D946GZIS	Section 1.2, page 15

### 1.1.2 Board Layout

Figure 1 shows the location of the major components.



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**Figure 1. Major Board Components**

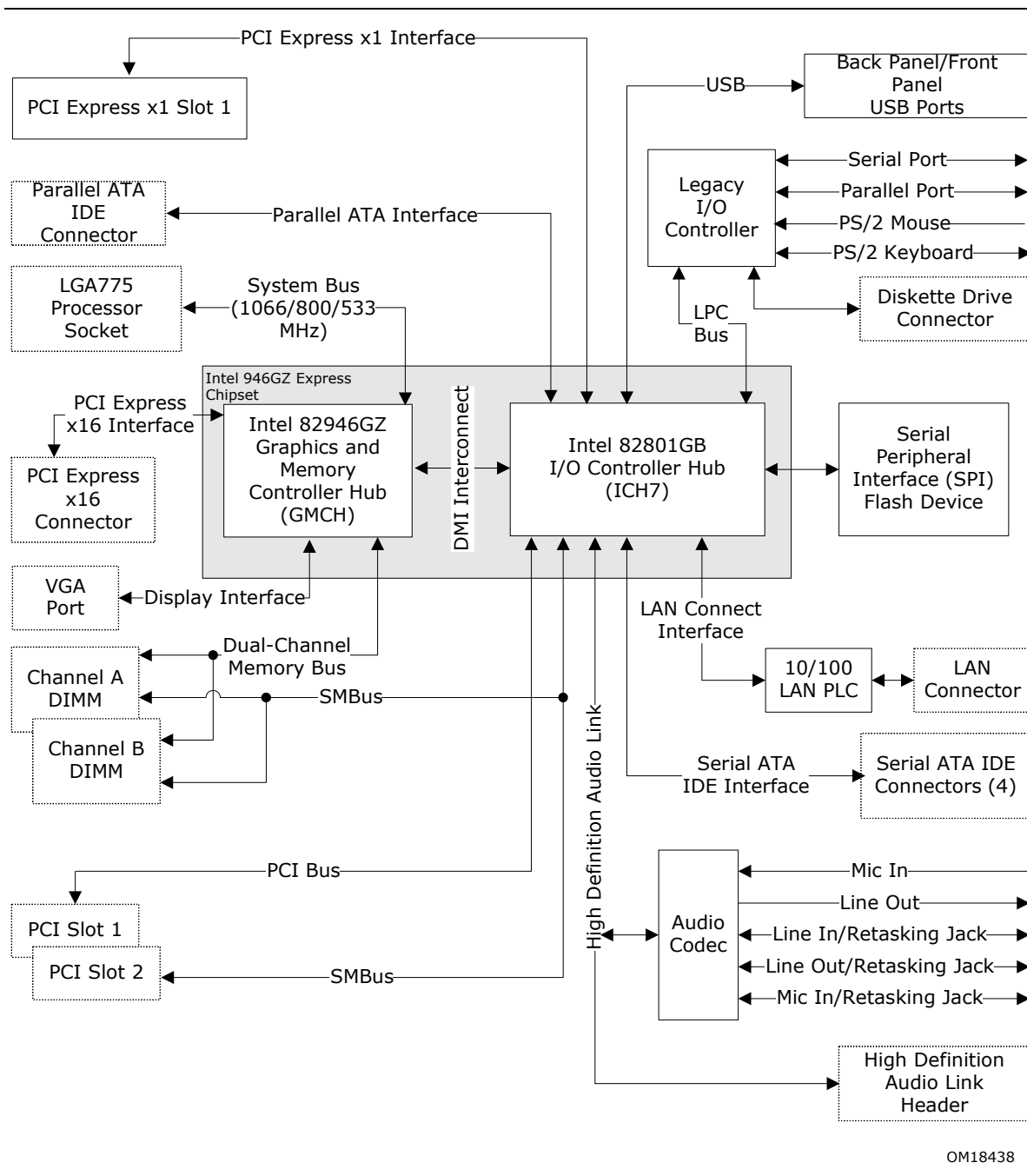
Table 2 lists the components identified in Figure 1.

**Table 2. Board Components Shown in Figure 1**

<b>Item/callout from Figure 1</b>	<b>Description</b>
A	Front panel audio header
B	PCI Express x1 connector
C	PCI Express x16 connector
D	Back panel connectors
E	Processor core power connector
F	Rear chassis fan header
G	LGA775 processor socket
H	Intel 82946GZ GMCH
I	Processor fan header
J	DIMM Channel A socket
K	DIMM Channel B socket
L	Main Power connector
M	Diskette drive connector
N	Parallel ATE IDE connector
O	Battery
P	Front chassis fan header
Q	Chassis intrusion header
R	Auxiliary front panel power LED header
S	Front panel header
T	Serial ATA connectors [4]
U	Intel 82801GB I/O Controller Hub (ICH7)
V	Front panel USB headers [2]
W	PCI Conventional bus add-in card connectors [2]
X	Speaker
Y	BIOS Setup configuration jumper block
Z	High Definition Audio Link header

### 1.1.3 Block Diagram

Figure 2 is a block diagram of the major functional areas.



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Figure 2. Block Diagram

## 1.2 Online Support

To find information about...	Visit this World Wide Web site:
Intel® Desktop Board D946GZIS under "Desktop Board Products" or "Desktop Board Support"	<a href="http://www.intel.com/design/motherbd">http://www.intel.com/design/motherbd</a>
Available configurations for the Desktop Board D946GZIS	<a href="http://support.intel.com/support/motherboards/desktop">http://support.intel.com/support/motherboards/desktop</a>
Processor data sheets	<a href="http://developer.intel.com/design/motherbd/is/is_available.htm">http://developer.intel.com/design/motherbd/is/is_available.htm</a>
ICH7 addressing	<a href="http://www.intel.com/products/index.htm">http://www.intel.com/products/index.htm</a>
Audio software and utilities	<a href="http://developer.intel.com/design/chipsets/datashts">http://developer.intel.com/design/chipsets/datashts</a>
LAN software and drivers	<a href="http://www.intel.com/design/motherbd">http://www.intel.com/design/motherbd</a>
Supported video modes	<a href="http://www.intel.com/design/motherbd/is/is_documentation.htm">http://www.intel.com/design/motherbd/is/is_documentation.htm</a>

## 1.3 Processor

The board is designed to support the following processors:

- Intel Core 2 Duo processor in an LGA775 socket with a 1066 or 800 MHz system bus
- Intel Pentium D processor in an LGA775 processor socket with an 800 or 533 MHz system bus
- Intel Pentium 4 processor in an LGA775 processor socket with an 800 or 533 MHz system bus
- Intel Celeron D processor in an LGA775 processor socket with a 533 MHz system bus

See the Intel web site listed below for the most up-to-date list of supported processors.

For information about...	Refer to:
Supported processors	<a href="http://www.intel.com/design/motherbd/is/is_proc.htm">http://www.intel.com/design/motherbd/is/is_proc.htm</a>



### CAUTION

*Use only the processors listed on web site above. Use of unsupported processors can damage the board, the processor, and the power supply.*



### INTEGRATOR'S NOTE

*Use only ATX12V-compliant power supplies.*

For information about	Refer to
Power supply connectors	Section 2.7.2.2, page 56

## 1.4 System Memory

The board has two DIMM sockets and support the following memory features:

- 1.8 V (only) DDR2 SDRAM DIMMs with gold-plated contacts
- Unbuffered, single-sided or double-sided DIMMs with the following restriction:  
Double-sided DIMMS with x16 organization are not supported.
- 4 GB maximum total system memory. Refer to Section 2.1.1 on page 43 for information on the total amount of addressable memory.
- Minimum total system memory: 128 MB
- Non-ECC DIMMs
- Serial Presence Detect
- DDR2 667 or DDR2 533 MHz SDRAM DIMMs

### NOTE

*To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.*

Table 3 lists the supported DIMM configurations.

**Table 3. Supported Memory Configurations**

<b>DIMM Type</b>	<b>DRAM Technology</b>	<b>Smallest usable DIMM (one x16 Single-sided DIMM)</b>	<b>Largest usable DIMM (one x8 Double-sided DIMM)</b>	<b>Maximum capacity with two identical x8 Double-sided DIMMs</b>
DDR2 533	256 Mbit	128 MB	512 MB	1 GB
DDR2 533	512 Mbit	256 MB	1 GB	2 GB
DDR2 533	1 Gbit	512 MB	2 GB	4 GB
DDR2 667	256 Mbit	128 MB	512 MB	1 GB
DDR2 667	512 Mbit	256 MB	1 GB	2 GB
DDR2 667	1 Gbit	512 MB	2 GB	4 GB



**⇒ NOTE**

Regardless of the DIMM type used, the memory frequency will either be equal to or less than the processor system bus frequency. For example, if DDR2 667 memory is used with a 533 MHz system bus frequency processor, the memory will operate at 533 MHz. Table 4 lists the resulting operating memory frequencies based on the combination of DIMMs and processors.

**Table 4. Memory Operating Frequencies**

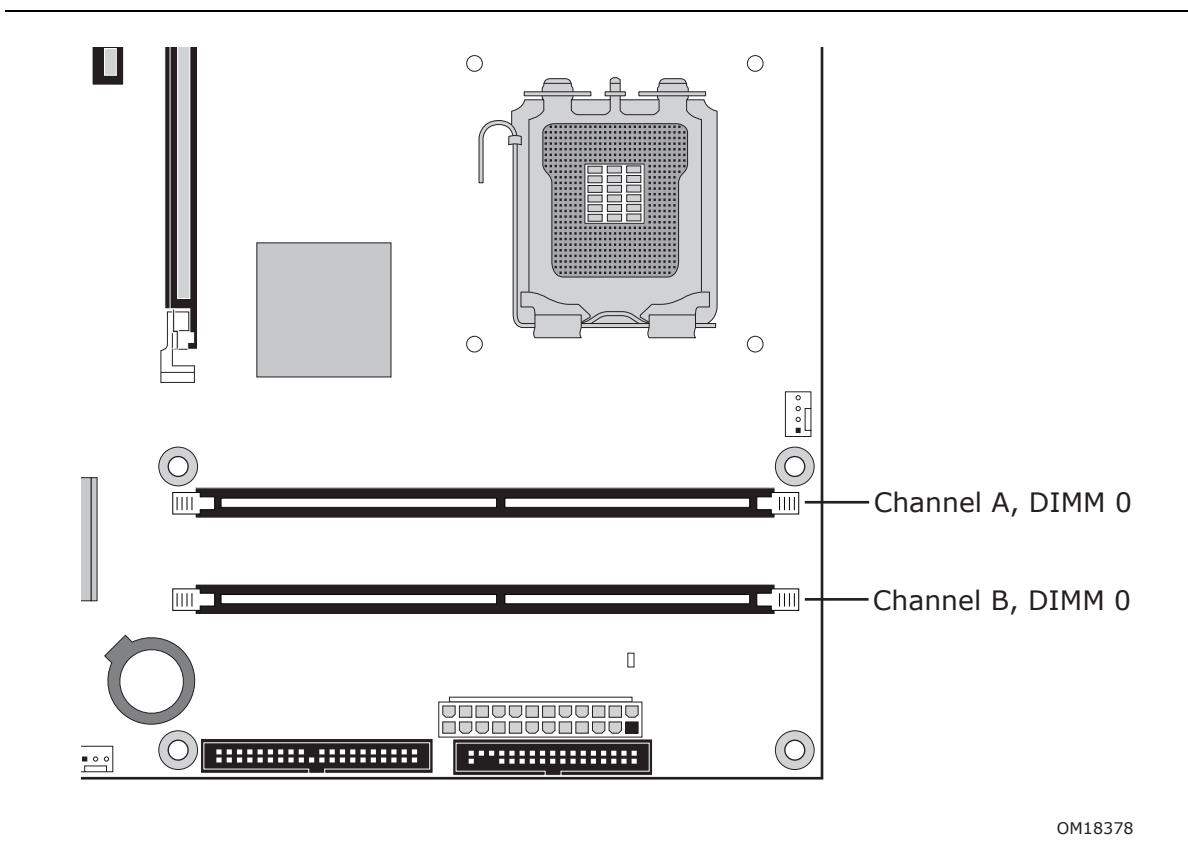
<b>DIMM Type</b>	<b>Processor system bus frequency</b>	<b>Resulting memory frequency</b>
DDR2 533	533 MHz	533 MHz
DDR2 533	800 MHz	533 MHz
DDR2 533	1066 MHz	533 MHz
DDR2 667	533 MHz	533 MHz
DDR2 667	800 MHz	667 MHz
DDR2 667	1066 MHz	667 MHz

### 1.4.1 Memory Configurations

The Intel 82946GZ GMCH supports two types of memory organization:

- **Dual channel (Interleaved) mode.** This mode offers the highest throughput for real world applications. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed DIMMs are used between channels, the slowest memory timing will be used.
- **Single channel (Asymmetric) mode.** This mode is equivalent to single channel bandwidth operation for real world applications. This mode is used when only a single DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speed DIMMs are used between channels, the slowest memory timing will be used.

Figure 3 illustrates the memory channel and DIMM configuration.

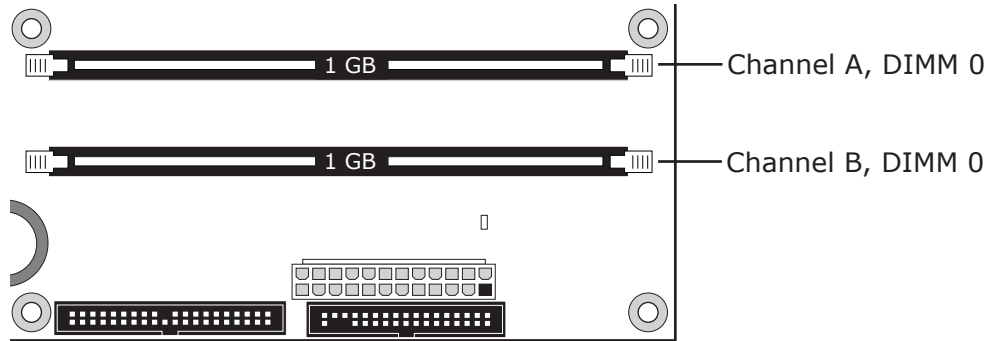


OM18378

Figure 3. Memory Channel and DIMM Configuration

### 1.4.1.1 Dual Channel (Interleaved) Mode Configuration

Figure 4 shows a dual channel configuration using two DIMMs. In this example, the DIMM sockets are populated with identical DIMMs.



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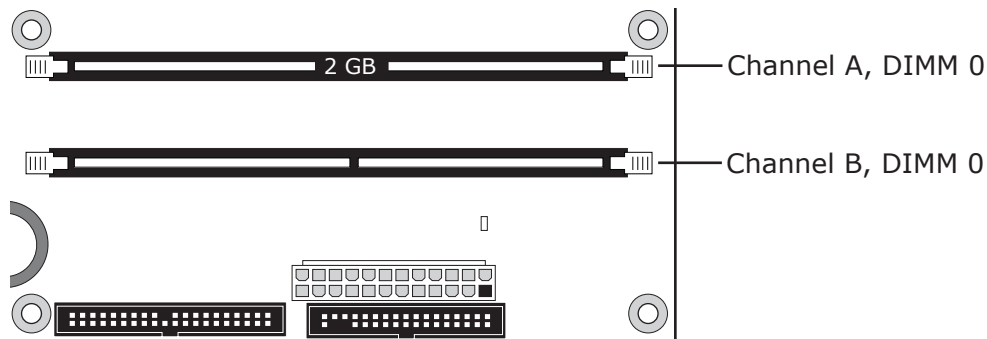
**Figure 4. Dual Channel (Interleaved) Mode Configuration with Two DIMMs**

### 1.4.1.2 Single Channel (Asymmetric) Mode Configurations

**NOTE**

*Dual channel (Interleaved) mode configurations provide the highest memory throughput.*

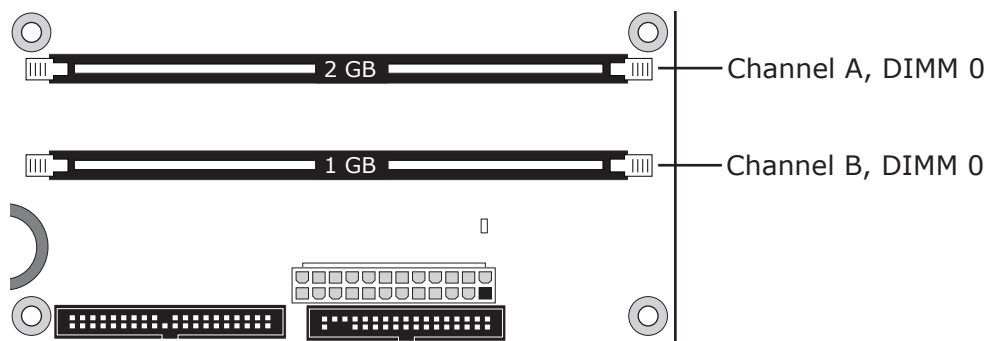
Figure 5 shows a single channel configuration using one DIMM. In this example, only Channel A is populated. Channel B is not populated.



OM18380

**Figure 5. Single Channel (Asymmetric) Mode Configuration with One DIMM**

Figure 6 shows a single channel configuration using two DIMMs. In this example, the capacity of the DIMM in Channel A does not equal the capacity of the DIMM in Channel B.



OM18381

**Figure 6. Single Channel (Asymmetric) Mode Configuration with Two DIMMs**

## 1.5 Intel® 946GZ Express Chipset

The Intel 946GZ Express chipset consists of the following devices:

- Intel 82946GZ Graphics and Memory Controller Hub (GMCH) with Direct Media Interface (DMI) interconnect
- Intel 82801GB I/O Controller Hub (ICH7) with DMI interconnect

The GMCH component provides interfaces to the CPU, memory, PCI Express, and the DMI interconnect. The component also provides integrated graphics capabilities supporting 3D, 2D and display capabilities. The ICH7 is a centralized controller for the board's I/O paths.

### For information about

### Refer to

The Intel 946GZ Express chipset

<http://developer.intel.com/>

Resources used by the chipset

Chapter 2

### 1.5.1 Intel 946GZ Graphics Subsystem

The Intel 946GZ Express chipset contains two separate, mutually exclusive graphics options. Either the GMA 3000 graphics controller (contained within the 82946GZ GMCH) is used, or a PCI Express x16 add-in card can be used. When a PCI Express x16 add-in card is installed, the GMA 3000 graphics controller is disabled.

#### 1.5.1.1 Intel® GMA 3000 Graphics Controller

The Intel GMA 3000 graphics controller features the following:

- 667 MHz core frequency
- High performance 3-D setup and render engine
- High quality texture engine
  - DX9\*/DX10 Compliant Hardware Shader Model 3.0
  - 32-bit full precision floating point operations
  - 128-bit floating point texture formats
  - Alpha and luminance maps
  - Texture color-keying/chroma-keying
  - Cubic environment reflection mapping
  - Enhanced texture blending functions
- 3D Graphics rendering enhancements
  - 1.3 dual texture GigaPixel/sec fill rate
  - 16 and 32 bit color
  - Maximum 3D supported resolution of 1600 x 1200 x 32 at 60 Hz
  - Vertex cache
  - Anti-aliased lines
  - OpenGL\* version 1.5 support with vertex buffer and EXT\_Shadow extensions

- 2D Graphics enhancements
  - 8, 16, and 32 bit color
  - Optimized 256-bit BLT engine
  - Color space conversion
  - Anti-aliased lines
- Video
  - Hardware motion compensation and iDCT for MPEG2
  - Software DVD at 30 fps full screen
- Display
  - Integrated 24-bit 400 MHz RAMDAC
  - Up to 2048 x 1536 at 75 Hz refresh (QXGA)
  - DDC2B compliant interface with Advanced Digital Display 2 or 2+ card (ADD2/ADD2+), support for TV-out/TV-in and DVI digital display connections
  - Supports flat panels up to 2048 x 1536 at 75 Hz (when in dual-channel mode) or digital CRT/HDTV at 1920 x 1080 at 85 Hz (with ADD2/MEC)
  - Two multiplexed SDVO port interfaces with 270 MHz pixel clocks using an ADD2/MEC card
- Dynamic Video Memory Technology (DVMT) support up to 256 MB
- Intel® Zoom Utility

### 1.5.1.2 Dynamic Video Memory Technology (DVMT)

DVMT enables enhanced graphics and memory performance through highly efficient memory utilization. DVMT ensures the most efficient use of available system memory for maximum 2-D/3-D graphics performance. Up to 256 MB of system memory can be allocated to DVMT on systems that have 512 MB or more of total system memory installed. Up to 128 MB can be allocated to DVMT on systems that have 256 MB but less than 512 MB of total installed system memory. Up to 64 MB can be allocated to DVMT when less than 256 MB of system memory is installed. DVMT returns system memory back to the operating system when the additional system memory is no longer required by the graphics subsystem.

DVMT will always use a minimal fixed portion of system physical memory (as set in the BIOS Setup program) for compatibility with legacy applications. An example of this would be when using VGA graphics under DOS. Once loaded, the operating system and graphics drivers allocate additional system memory to the graphics buffer as needed for performing graphics functions.

#### **NOTE**

*The use of DVMT requires operating system driver support.*

### 1.5.1.3 Configuration Modes

A list of supported modes for the Intel GMA 3000 graphics controller is available as a downloadable document.

For information about	Refer to
Supported video modes for the board	Section 1.2, page 15

### 1.5.1.4 Advanced Digital Display (ADD2/ADD2+) Card Support

The GMCH routes two multiplexed SDVO ports that are each capable of driving up to a 200 MHz pixel clock to the PCI Express x16 connector. The SDVO ports can be paired for a dual channel configuration to support up to a 400 MHz pixel clock. When an ADD2/ADD2+ card is detected, the Intel GMA 3000 graphics controller is enabled and the PCI Express x16 connector is configured for SDVO mode. SDVO mode enables the SDVO ports to be accessed by the ADD2/ADD2+ card. An ADD2/ADD2+ card can either be configured to support simultaneous display with the primary VGA display or can be configured to support dual independent display as an extended desktop configuration with different color depths and resolutions. ADD2/ADD2+ cards can be designed to support the following configurations:

- TV-Out (composite video)
- Transition Minimized Differential Signaling (TMDS) for DVI 1.0
- Low Voltage Differential Signaling (LVDS)
- Single device operating in dual channel mode
- VGA output
- HDTV output
- HDMI/UDI support (when used with the HD Audio Link)

## 1.5.2 USB

The board supports up to eight USB 2.0 ports, supports UHCI and EHCI, and uses UHCI- and EHCI-compatible drivers.

The ICH7 provides the USB controller for all ports. The port arrangement is as follows:

- Four ports are implemented with stacked back panel connectors
- Four ports are routed to two separate front panel USB headers

### NOTE

*Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.*

For information about	Refer to
The location of the USB connectors on the back panel	Figure 13, page 51
The location of the front panel USB headers	Figure 14, page 52

### 1.5.3 Serial ATA Interfaces

The board provides four Serial ATA (SATA) connectors, which support one device per connector.

#### 1.5.3.1 Serial ATA Support

The ICH7's Serial ATA controller offers four independent Serial ATA ports with a theoretical maximum transfer rate of 3 Gbits/sec per port. One device can be installed on each port for a maximum of four Serial ATA devices. A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows\* XP and Windows 2000 operating systems.

#### **NOTE**

*Many Serial ATA drives use new low-voltage power connectors and require adaptors or power supplies equipped with low-voltage power connectors.*

For more information, see: <http://www.serialata.org/>.

<b>For information about</b>	<b>Refer to</b>
The location of the Serial ATA connectors	Figure 14, page 52



## 1.5.4 Parallel IDE Interface

The Parallel ATA IDE controller has one bus-mastering Parallel ATA IDE interface. The Parallel ATA IDE interface supports the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

### NOTE

*ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.*

The Parallel ATA IDE interface also supports ATAPI devices (such as CD-ROM drives) and ATA devices. The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

#### **For information about**

The location of the Parallel ATA IDE connector

#### **Refer to**

Figure 14, page 52

## 1.5.5 Real-Time Clock, CMOS SRAM, and Battery

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to  $\pm 13$  minutes/year at 25 °C with 3.3 VSB applied.

### **NOTE**

*If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.*

When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate. Replace the battery with an equivalent one. Figure 1 on page 12 shows the location of the battery.



### **CAUTION**

*Risk of explosion if the battery is replaced with an incorrect type. Batteries should be recycled where possible. Disposal of used batteries must be in accordance with local environmental regulations.*



### **PRECAUTION**

*Risque d'explosion si la pile usagée est remplacée par une pile de type incorrect. Les piles usagées doivent être recyclées dans la mesure du possible. La mise au rebut des piles usagées doit respecter les réglementations locales en vigueur en matière de protection de l'environnement.*



### **FORHOLDSREGEL**

*Ekspløsningsfare, hvis batteriet erstattes med et batteri af en forkert type. Batterier bør om muligt genbruges. Bortskaffelse af brugte batterier bør foregå i overensstemmelse med gældende miljølovgivning.*



### **OBS!**

*Det kan oppstå eksplosjonsfare hvis batteriet skiftes ut med feil type. Brukte batterier bør kastes i henhold til gjeldende miljølovgivning.*



### **VIKTIGT!**

*Risk för explosion om batteriet ersätts med felaktig batterityp. Batterier ska kasseras enligt de lokala miljövårdsbestämmelserna.*



### **VARO**

*Räjähdyksvaara, jos pariston tyyppi on väärä. Paristot on kierrätettävä, jos se on mahdollista. Käytetyt paristot on hävitettävä paikallisten ympäristömääräysten mukaisesti.*



### **VORSICHT**

*Bei falschem Einsetzen einer neuen Batterie besteht Explosionsgefahr. Die Batterie darf nur durch denselben oder einen entsprechenden, vom Hersteller empfohlenen Batterietyp ersetzt werden. Entsorgen Sie verbrauchte Batterien den Anweisungen des Herstellers entsprechend.*



### **AVVERTIMENTO**

*Esiste il pericolo di un esplosione se la pila non viene sostituita in modo corretto. Utilizzare solo pile uguali o di tipo equivalente a quelle consigliate dal produttore. Per disfarsi delle pile usate, seguire le istruzioni del produttore.*



### **PRECAUCIÓN**

*Existe peligro de explosión si la pila no se cambia de forma adecuada. Utilice solamente pilas iguales o del mismo tipo que las recomendadas por el fabricante del equipo. Para deshacerse de las pilas usadas, siga igualmente las instrucciones del fabricante.*



### **WAARSCHUWING**

*Er bestaat ontploffingsgevaar als de batterij wordt vervangen door een onjuist type batterij. Batterijen moeten zoveel mogelijk worden gerecycled. Houd u bij het weggooien van gebruikte batterijen aan de plaatselijke milieuwetgeving.*



### **ATENÇÃO**

*Haverá risco de explosão se a bateria for substituída por um tipo de bateria incorreto. As baterias devem ser recicladas nos locais apropriados. A eliminação de baterias usadas deve ser feita de acordo com as regulamentações ambientais da região.*



### **AŚCIAROŻZNAŚĆ**

*Існуе рызыка выбуху, калі заменены акумулятар неправільнага тыпу. Акумулятары павінны, па магчымасці, перепрацоўвацца. Пазбаўляцца ад старых акумулятараў патрэбна згодна з мясцовым заканадаўствам па экалогіі.*



### **UPOZORNĚNÍ**

*V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.*



### **Προσοχή**

*Υπάρχει κίνδυνος για έκρηξη σε περίπτωση που η μπαταρία αντικατασταθεί από μία λανθασμένου τύπου. Οι μπαταρίες θα πρέπει να ανακυκλώνονται όταν κάτι τέτοιο είναι δυνατό. Η απόρριψη των χρησιμοποιημένων μπαταριών πρέπει να γίνεται σύμφωνα με τους κατά τόπο περιβαλλοντικούς κανονισμούς.*



### VIGYAZAT

*Ha a telepet nem a megfelelő típusú telepre cseréli, az felrobbanhat. A telepeket lehetőség szerint újra kell hasznosítani. A használt telepeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.*



### 注意

異なる種類の電池を使用すると、爆発の危険があります。リサイクルが可能な地域であれば、電池をリサイクルしてください。使用後の電池を破棄する際には、地域の環境規制に従ってください。



### AWAS

*Risiko letupan wujud jika bateri digantikan dengan jenis yang tidak betul. Bateri sepatutnya dikitar semula jika boleh. Pelupusan bateri terpakai mestilah mematuhi peraturan alam sekitar tempatan.*



### OSTRZEŻENIE

*Istnieje niebezpieczeństwo wybuchu w przypadku zastosowania niewłaściwego typu baterii. Zużyte baterie należy w miarę możliwości utylizować zgodnie z odpowiednimi przepisami ochrony środowiska.*



### PRECAUȚIE

*Risc de explozie, dacă bateria este înlocuită cu un tip de baterie necorespunzător. Bateriile trebuie reciclate, dacă este posibil. Depozitarea bateriilor uzate trebuie să respecte reglementările locale privind protecția mediului.*



### ВНИМАНИЕ

*При использовании батареи несоответствующего типа существует риск ее взрыва. Батареи должны быть утилизированы по возможности. Утилизация батарей должна проводиться по правилам, соответствующим местным требованиям.*



### UPOZORNENIE

*Ak batériu vymeníte za nesprávny typ, hrozí nebezpečenstvo jej výbuchu. Batérie by sa mali podľa možnosti vždy recyklovať. Likvidácia použitých batérií sa musí vykonávať v súlade s miestnymi predpismi na ochranu životného prostredia.*



### POZOR

*Zamenjava baterije z baterijo drugačnega tipa lahko povzroči eksplozijo. Če je mogoče, baterije reciklirajte. Rabljene baterije zavrzite v skladu z lokalnimi okoljevarstvenimi predpisi.*



### คำเตือน

*ระวังการระเบิดที่เกิดจากเปลี่ยนแบตเตอรี่ผิดประเภท หากเป็นไปได้ ควรนำแบตเตอรี่ไปรีไซเคิล การทิ้งแบตเตอรี่ใช้แล้วต้องเป็นไปตามกฎข้อบังคับด้านสิ่งแวดล้อมของท้องถิ่น.*

**UYARI**

*Yanlış türde pil takıldığında patlama riski vardır. Piller mümkün olduğunda geri dönüştürülmelidir. Kullanılmış piller, yerel çevre yasalarına uygun olarak atılmalıdır.*

**ОСТОРОГА**

*Використовуйте батареї правильного типу, інакше існуватиме ризик вибуху. Якщо можливо, використані батареї слід утилізувати. Утилізація використаних батарей має бути виконана згідно місцевих норм, що регулюють охорону довкілля.*

**UPOZORNĚNÍ**

*V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.*

**ETTEVAATUST**

*Kui patarei asendatakse uue ebasobivat tüüpi patareiga, võib tekkida plahvatusoht. Tühjad patareid tuleb võimaluse korral viia vastavasse kogumispunkti. Tühjade patareide äraviskamisel tuleb järgida kohalikke keskkonnakaitse alaseid reegleid.*

**FIGYELMEZTETÉS**

*Ha az elemet nem a megfelelő típusúra cseréli, felrobbanhat. Az elemeket lehetőség szerint újra kell hasznosítani. A használt elemeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.*

**UZMANĪBU**

*Pastāv eksplozijas risks, ja baterijas tiek nomainītas ar nepareiza veida baterijām. Ja iespējams, baterijas vajadzētu nodot attiecīgos pieņemšanas punktus. Bateriju izmešanai atkritumos jānotiek saskaņā ar vietējiem vides aizsardzības noteikumiem.*

**DĒMESIO**

*Naudojant netinkamo tipo baterijas įrenginys gali sprogti. Kai tik įmanoma, baterijas reikia naudoti pakartotinai. Panaudotas baterijas išmesti būtina pagal vietinius aplinkos apsaugos nuostatus.*

**ATTENZJONI**

*Riskju ta' splużjoni jekk il-batterija tinbidel b'tip ta' batterija mhux korrett. Il-batteriji għandhom jiġu riċiklati fejn hu possibbli. Ir-rimi ta' batteriji użati għandu jsir skond ir-regolamenti ambjentali lokali.*

**OSTRZEŻENIE**

*Ryzyko wybuchu w przypadku wymiany na baterie niewłaściwego typu. W miarę możliwości baterie należy poddać recyklingowi. Zużytych baterii należy pozbywać się zgodnie z lokalnie obowiązującymi przepisami w zakresie ochrony środowiska.*

## 1.6 Legacy I/O Controller

The I/O controller provides the following features:

- One serial port
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.44 MB or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

### 1.6.1 Serial Port

The board has one serial port connector located on the back panel. The serial port supports data transfers at speeds up to 115.2 kbits/sec with BIOS support.

For information about	Refer to
The location of the serial port connector	Figure 13, page 51

### 1.6.2 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. Use the BIOS Setup program to set the parallel port mode.

For information about	Refer to
The location of the parallel port connector	Figure 13, page 51

### 1.6.3 Diskette Drive Controller

The I/O controller supports one diskette drive. Use the BIOS Setup program to configure the diskette drive interface.

For information about	Refer to
The location of the diskette drive connector	Figure 14, page 52

### 1.6.4 Keyboard and Mouse Interface

The PS/2 keyboard and mouse connectors are located on the back panel.

#### NOTE

*The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.*

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 13, page 51

## 1.7 Audio Subsystem

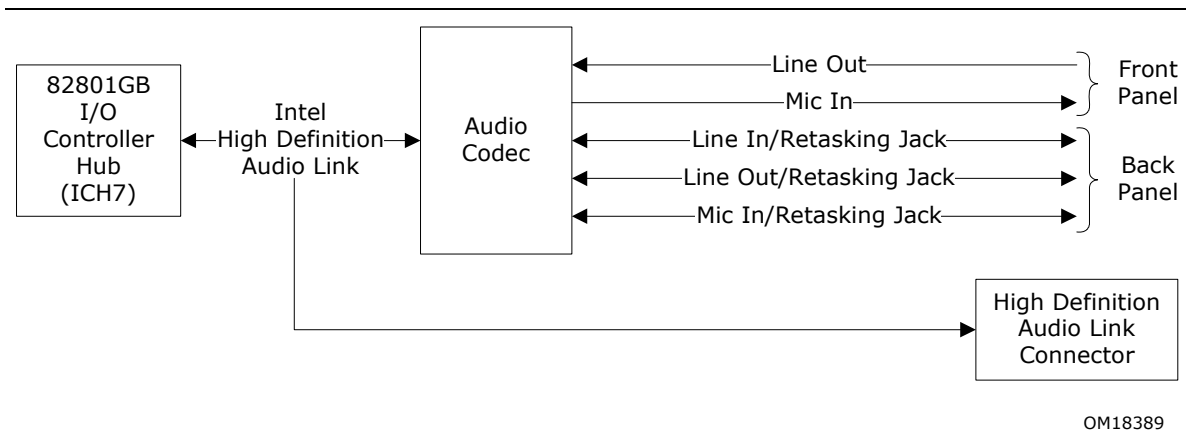
The onboard audio subsystem consists of the following:

- Intel 82801GB ICH7
- Analog Devices ADI1988A (or Sigmatel STAC9227) audio codec
- Back panel audio connectors
- Component-side audio headers

The audio subsystem supports the following features:

- Advanced jack sense for the back panel audio jacks that enables the audio codec to recognize the device that is connected to an audio port. Within hardware constraints, the back panel audio jacks are capable of retasking according to the user's definition, or can be automatically switched depending on the recognized device type.
- Stereo input and output for all back panel jacks
- Line out and Mic in functions for front panel audio jacks
- A signal-to-noise (S/N) ratio of 95 dB
- SLIC Voice over IP (VoIP) support using the High Definition Audio link header

Figure 7 is a block diagram of the audio subsystem.



**Figure 7. 6-Channel (5.1) Audio Subsystem Block Diagram**

## 1.7.1 Audio Subsystem Software

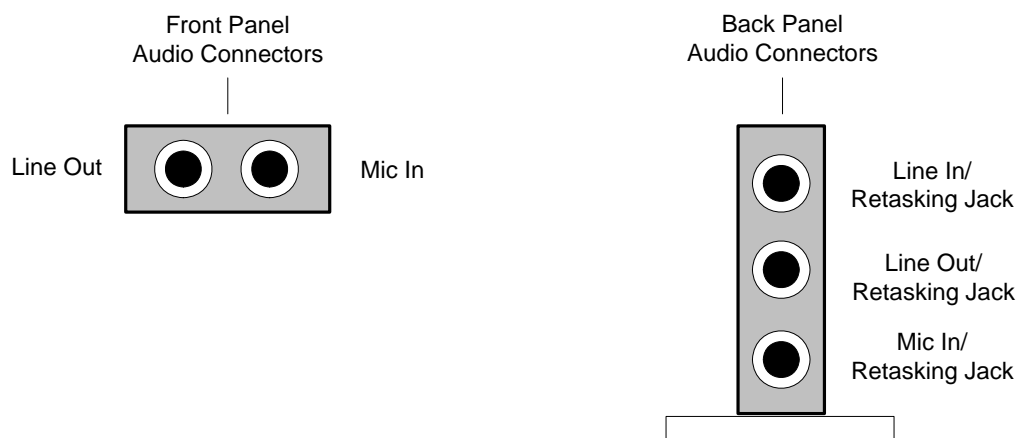
Audio software and drivers are available from Intel’s World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.2, page 15

## 1.7.2 Audio Connectors and Headers

The board contains audio connectors on the back panel and audio headers on the component side of the board. The front panel audio header provides mic in and line out signals for the front panel. Microphone bias is supported for both the front and back panel microphone connectors.

The back panel audio connectors are configurable through the audio device drivers. The available configurable audio ports are shown in Figure 8.



OM17560

**Figure 8. Front/Back Panel Audio Connector Options**

For information about	Refer to
The location of the front panel audio header	Figure 14, page 52
The signal names of the front panel audio header	Table 16, page 53
The location of the HD Audio Link header	Figure 14, page 52
The signal names of the HD Audio Link header	Table 21, page 54
The back panel audio connectors	Section 2.7.1, page 51



## 1.8 LAN Subsystem

The LAN subsystem consists of the following:

- Intel 82562G Platform LAN Connect (PLC) device for 10/100 Mbits/sec Ethernet LAN connectivity
- Intel 82801GB ICH7
- RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:

- CSMA/CD protocol engine
- LAN connect interface between ICH7 and PLC device
- PCI Conventional bus power management
  - Supports ACPI technology
  - Supports LAN wake capabilities

### 1.8.1 Intel® 82562G PLC Device

The Intel 82562G PLC device supports the following features:

- Basic 10/100 Ethernet LAN connectivity
- Full device driver compatibility
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

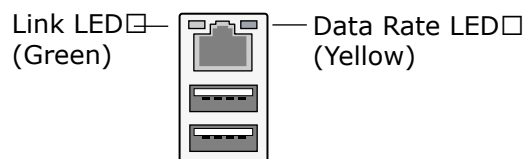
### 1.8.2 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.2, page 15

### 1.8.3 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 9 below).



OM18388

**Figure 9. LAN Connector LED Locations**

Table 5 describes the LED states when the board is powered up and the LAN subsystem is operating.

**Table 5. LAN Connector LED States**

LED	LED Color	LED State	Condition
Link	Green	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring
Data Rate	Yellow	Off	10 Mbits/sec data rate is selected.
		On	100 Mbits/sec data rate is selected.

## 1.9 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Fan monitoring and control
- Thermal and voltage monitoring
- Chassis intrusion detection

### 1.9.1 Hardware Monitoring and Fan Control

The features of the hardware monitoring and fan control include:

- Power supply monitoring of four voltages (+5 V, +12 V, +3.3 VSB, and +VCCP) to detect levels above or below acceptable values
- Thermally monitored closed-loop fan control, for all three fans, that can adjust the fan speed or switch the fans on or off as needed

### 1.9.2 Fan Monitoring

Fan monitoring can be implemented using Intel Desktop Utilities or third-party software.

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**For information about**

The functions of the fan headers

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**Refer to**

Section 1.10.2.2, page 39

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### 1.9.3 Chassis Intrusion and Detection

The board supports a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion header. When the chassis cover is removed, the mechanical switch is in the closed position.

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**For information about**

The location of the chassis intrusion header

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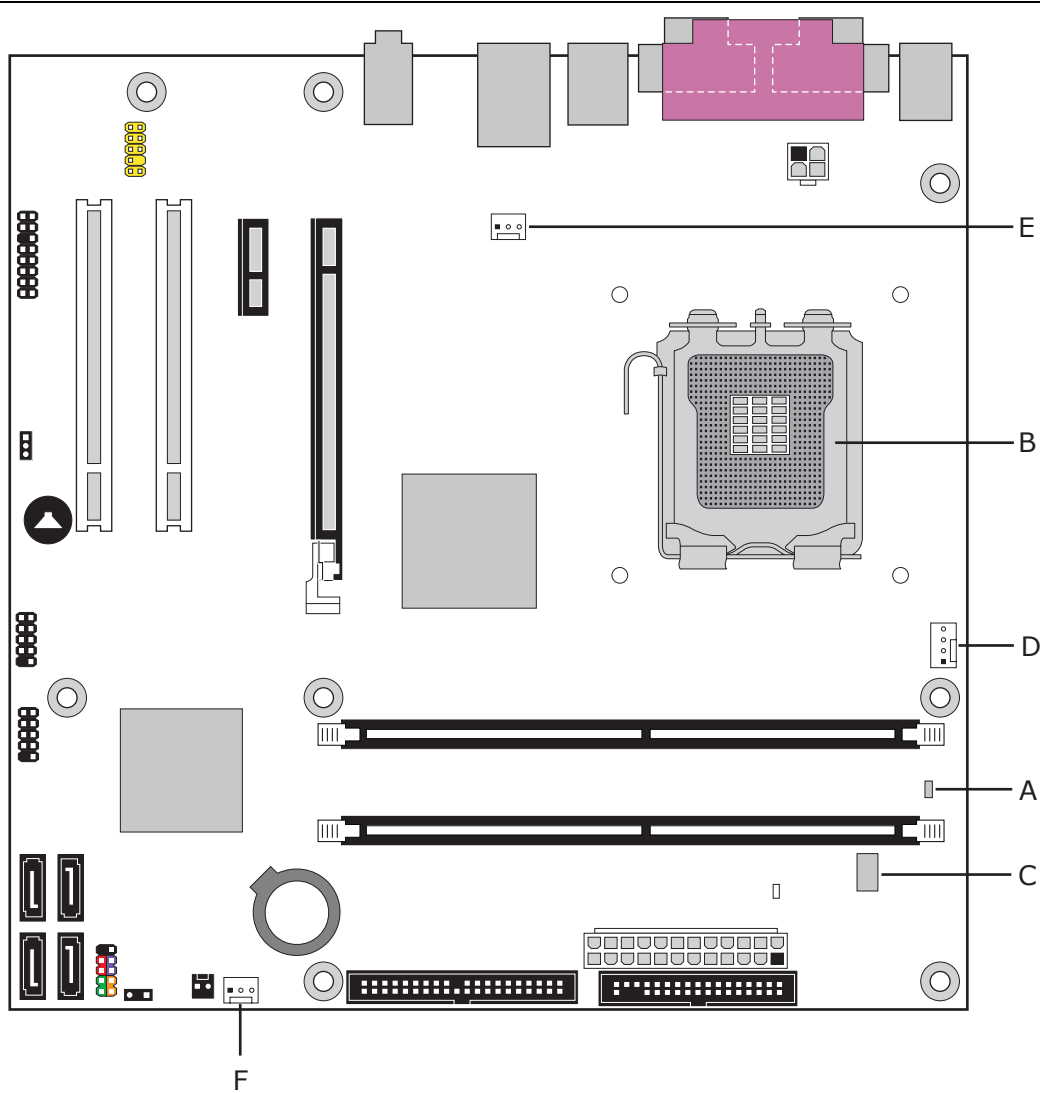
**Refer to**

Figure 14, page 52

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### 1.9.4 Thermal Monitoring

Figure 10 shows the locations of the thermal sensors and fan headers.



OM18382

Item	Description
A	Remote thermal sensor
B	Thermal diode, located on processor die
C	Hardware monitoring and fan control ASIC
D	Processor fan
E	Rear chassis fan
F	Front chassis fan

**Figure 10. Thermal Sensors and Fan Headers**

## 1.10 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan headers
  - LAN wake capabilities
  - Instantly Available PC technology
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event signal (PME#) wake-up support

### 1.10.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 8 on page 38)
- Support for a front panel power and sleep mode switch

Table 6 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

**Table 6. Effects of Pressing the Power Switch**

<b>If the system is in this state...</b>	<b>...and the power switch is pressed for</b>	<b>...the system enters this state</b>
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

### 1.10.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 7 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

**Table 7. Power States and Targeted System Power**

<b>Global States</b>	<b>Sleeping States</b>	<b>Processor States</b>	<b>Device States</b>	<b>Targeted System Power</b> (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 52.5 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off. AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

### 1.10.1.2 Two-Watt Standby

In 2001, the U.S. government issued an executive order requiring a reduction in power for appliances and personal computers. This board meets that requirement by operating at 1.5 W (or less) in S5 (Standby) mode. Two-Watt operation applies only to the S5 state when the computer is turned off, but still connected to AC power. Two-Watt operation does not apply to the S3 (Suspend to RAM) or S4 (Suspend to disk) states.

Newer energy-efficient power supplies using less than 0.5 W (in Standby mode) may also be needed to achieve this goal.

### 1.10.1.3 Wake-up Devices and Events

Table 8 lists the devices or specific events that can wake the computer from specific states.

**Table 8. Wake-up Devices and Events**

These devices/events can wake up the computer...	...from this state
LAN	S1, S3, S4, S5 (Note)
PME# signal	S1, S3, S4, S5 (Note)
Power switch	S1, S3, S4, S5
PS/2 devices	S1, S3
RTC alarm	S1, S3, S4, S5
Serial port	S1, S3
USB	S1, S3
WAKE# signal	S1, S3, S4, S5

Note: For LAN and PME# signal, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.

#### NOTE

*The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.*

### 1.10.2 Hardware Support

#### CAUTION

*Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.*

The board provides several power management hardware features, including:

- Power connector
- Fan headers
- LAN wake capabilities
- Instantly Available PC technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# signal wake-up support
- WAKE# signal wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal).

## ⇒ NOTE

*The use of Resume on Ring and Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.*

### 1.10.2.1 Power Connector

ATX12V-compliant power supplies can turn off the system power through system control. When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the main power connector	Figure 14, page 52
The signal names of the main power connector	Table 23, page 56

### 1.10.2.2 Fan Headers

The function/operation of the fan headers is as follows:

- The fans are on when the board is in the S0 or S1 state.
- The fans are off when the board is off or in the S3, S4, or S5 state.
- Each fan header is wired to a fan tachometer input of the hardware monitoring and fan control device.
- All fan headers support closed-loop fan control that can adjust the fan speed or switch the fan on or off as needed.
- All fan headers have a +12 V DC connection.

For information about	Refer to
The locations of the fan headers and thermal sensors	Figure 10, page 35
The signal names of the processor fan header	Table 18, page 54
The signal names of the chassis fan headers	Table 17, page 53

### 1.10.2.3 LAN Wake Capabilities



#### CAUTION

*For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.*

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet\* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the board supports LAN wake capabilities with ACPI in the following ways:

- The PCI Express WAKE# signal
- The PCI bus PME# signal for PCI 2.3 compliant LAN designs
- The onboard LAN subsystem

### 1.10.2.4 Instantly Available PC Technology



#### CAUTION

*For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.*

Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 8 on page 38 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification*. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.3 compliant add-in cards and drivers.

### 1.10.2.5 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from ACPI S1 or S3 states
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation



### 1.10.2.6 Wake from USB

USB bus activity wakes the computer from ACPI S1 or S3 states.

#### NOTE

*Wake from USB requires the use of a USB peripheral that supports Wake from USB.*

### 1.10.2.7 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1 or S3 state.

### 1.10.2.8 PME# Signal Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with Wake on PME enabled in BIOS).

### 1.10.2.9 WAKE# Signal Wake-up Support

When the WAKE# signal on the PCI Express bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state.

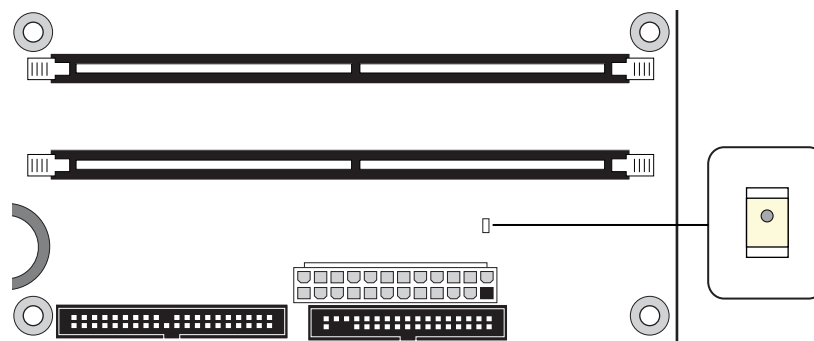
### 1.10.2.10 +5 V Standby Power Indicator LED

The +5 V standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 11 shows the location of the standby power indicator LED.



#### CAUTION

*If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.*



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**Figure 11. Location of the Standby Power Indicator LED**



## 2 Technical Reference

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### What This Chapter Contains

2.1	Memory Map.....	43
2.2	DMA Channels.....	45
2.3	Fixed I/O Map .....	46
2.4	PCI Configuration Space Map .....	47
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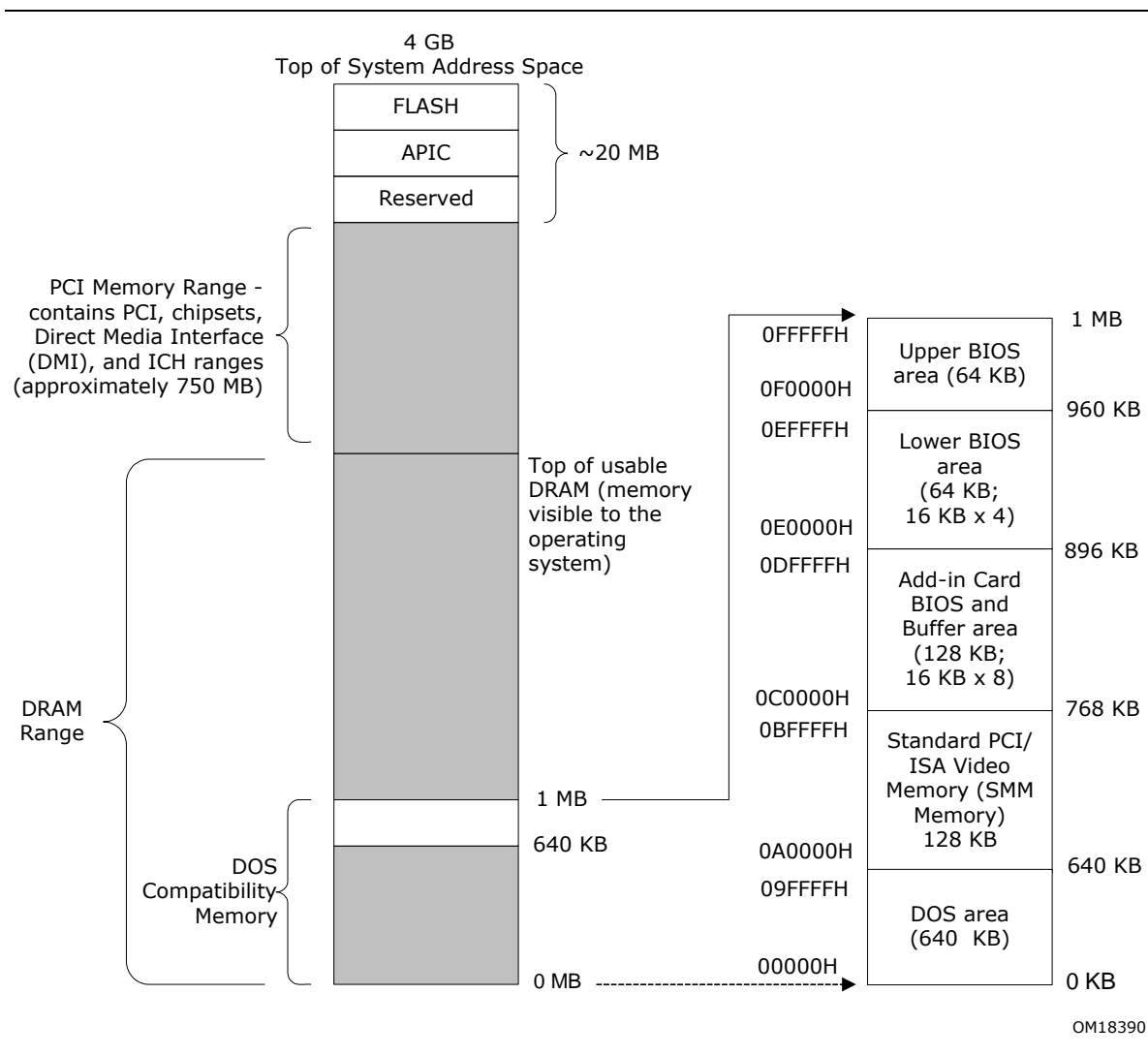
### 2.1 Memory Map

#### 2.1.1 Addressable Memory

The board utilizes 4 GB of addressable system memory. Typically the address space that is allocated for PCI Conventional bus add-in cards, PCI Express configuration space, BIOS (SPI Flash), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 4 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- BIOS/ SPI Flash (4 Mbits)
- Local APIC (19 MB)
- Digital Media Interface (40 MB)
- Front side bus interrupts (17 MB)
- PCI Express configuration space (256 MB)
- MCH base address registers, internal graphics ranges, PCI Express ports (up to 512 MB)
- Memory-mapped I/O that is dynamically allocated for PCI Conventional and PCI Express add-in cards
- Base graphics memory support (8 MB)

The amount of installed memory that can be used will vary based on add-in cards and BIOS settings. Figure 12 shows a schematic of the system memory map. All installed system memory can be used when there is no overlap of system addresses.



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Figure 12. Detailed System Memory Address Map

Table 9 lists the system memory map.

**Table 9. System Memory Map**

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 4194304 K	100000 - FFFFFFFF	4095 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Potential available high DOS memory (open to the PCI bus). Dependent on video adapter used.
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

## 2.2 DMA Channels

**Table 10. DMA Channels**

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP or EPP)
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

## 2.3 Fixed I/O Map

**Table 11. I/O Map**

Address (hex)	Size	Description
0000 - 00FF	256 bytes	Used by the Desktop Board D946GZIS. Refer to the ICH7 data sheet for dynamic addressing information.
01F0 - 01F7	8 bytes	Primary Parallel ATE IDE channel command block
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4
02F8 - 02FF (Note 1)	8 bytes	COM2
0378 - 037F	8 bytes	LPT1
03B0 - 03BB	12 bytes	Intel 82946GZ GMCH
03C0 - 03DF	32 bytes	Intel 82946GZ GMCH
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette channel
03F4 - 03F7	4 bytes	Primary Parallel ATA IDE channel control block
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI configuration address register
0CF9 (Note 3)	1 byte	Reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary Parallel ATA IDE bus master registers

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

### NOTE

*Some additional I/O addresses are not available due to ICH7 address aliasing. The ICH7 data sheet provides more information on address aliasing.*

#### **For information about**

Obtaining the ICH7 data sheet

#### **Refer to**

Section 1.2 on page 15

## 2.4 PCI Configuration Space Map

**Table 12. PCI Configuration Space Map**

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82946GZ component
00	01	00	PCI Express x16 graphics port <sup>(Note 1)</sup>
00	02	00	Integrated graphics controller
00	1B	00	Intel High Definition Audio Controller
00	1C	00	PCI Express port 1
00	1C	01	PCI Express port 2
00	1C	02	PCI Express port 3
00	1C	03	PCI Express port 4
00	1C	04	PCI Express port 5
00	1D	00	USB UHCI controller 1
00	1D	01	USB UHCI controller 2
00	1D	02	USB UHCI controller 3
00	1D	03	USB UHCI controller 4
00	1D	07	EHCI controller #1
00	1E	00	PCI bridge
00	1F	00	PCI controller
00	1F	01	Parallel ATA IDE controller
00	1F	02	Serial ATA controller #1
00	1F	03	SMBus controller
(Note 2)	08	00	LAN controller
(Note 2)	00	00	PCI Conventional bus connector 1
(Note 2)	01	00	PCI Conventional bus connector 2
01	00	00	PCI Express Video Controller <sup>(Note 1)</sup>

**Notes:**

1. Present only when a PCI Express x16 graphics card is installed.
2. Bus number is dynamic and can change based on add-in cards used.

## 2.5 Interrupts

The interrupts can be routed through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the ICH7 component. The PIC is supported in Windows 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and supports a total of 24 interrupts.

**Table 13. Interrupts**

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option)/User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for ICH7 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE/Serial ATA (if present, else user available)
15	Secondary IDE/Serial ATA (if present, else user available)
16 (Note 2)	USB UHCI controller 1 / USB UHCI controller 4 (through PIRQA)
17 (Note 2)	AC '97 audio/modem/User available (through PIRQB)
18 (Note 2)	ICH7 USB controller 3 (through PIRQC)
19 (Note 2)	ICH7 USB controller 2 (through PIRQD)
20 (Note 2)	ICH7 LAN (through PIRQE)
21 (Note 2)	User available (through PIRQF)
22 (Note 2)	User available (through PIRQG)
23 (Note 2)	ICH7 USB 2.0 EHCI controller/User available (through PIRQH)

Notes:

1. Default, but can be changed to another IRQ.
2. Available in APIC mode only.



## 2.6 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH7 has eight Programmable Interrupt Request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the board and therefore share the same interrupt. Table 14 shows an example of how the PIRQ signals are routed.

**Table 14. PCI Interrupt Routing Map**

PCI Interrupt Source	ICH7 PIRQ Signal Name							
	PIRQA	PIRQB	PIRQC	PIRQD	PIRQE	PIRQF	PIRQG	PIRQH
SMBus controller				INTC				
ICH7 LAN					INTA			
PCI bus connector 1					INTD	INTA	INTB	INTC
PCI bus connector 2					INTC	INTB	INTA	INTD

 **NOTE**

*In PIC mode, the ICH7 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. Refer to Table 13 for the allocation of PIRQ lines to IRQ signals in APIC mode.*

*PCI interrupt assignments to USB ports and Serial ATA ports are dynamic.*

## 2.7 Connectors and Headers



### CAUTION

*Only the following connectors have overcurrent protection: Back panel and front panel USB, PS/2, and VGA.*

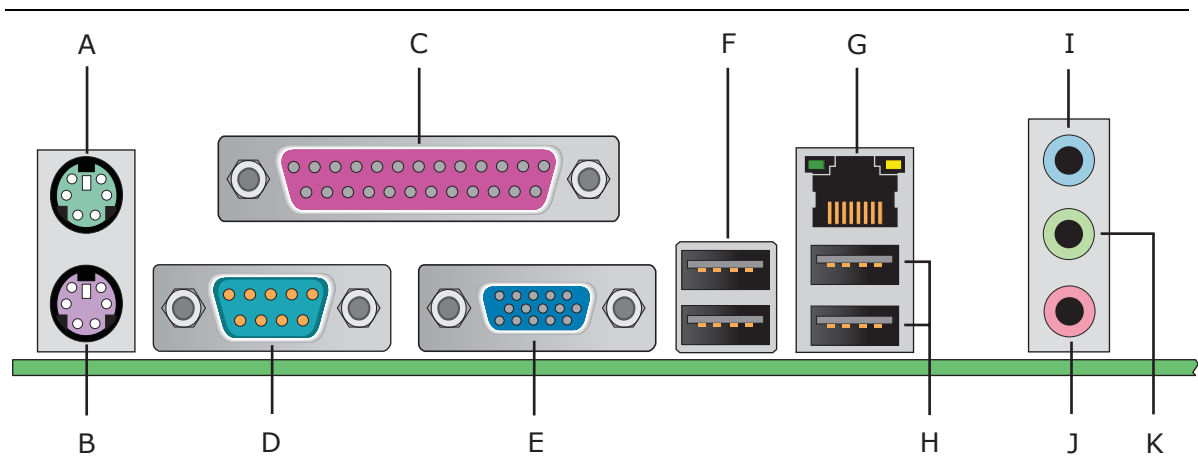
*The other internal connectors/headers are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors/headers to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.*

This section describes the board's connectors and headers. The connectors and headers can be divided into these groups:

- Back panel I/O connectors (see page 51)
- Component-side connectors and headers (see page 52)

## 2.7.1 Back Panel Connectors

Figure 13 shows the location of the back panel connectors.



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Item	Description
A	PS/2 mouse port
B	PS/2 keyboard port
C	Parallel port
D	VGA port
E	Serial port
F	USB ports [2]
G	LAN
H	USB ports [2]
I	Audio line in
J	Mic in
K	Audio line out

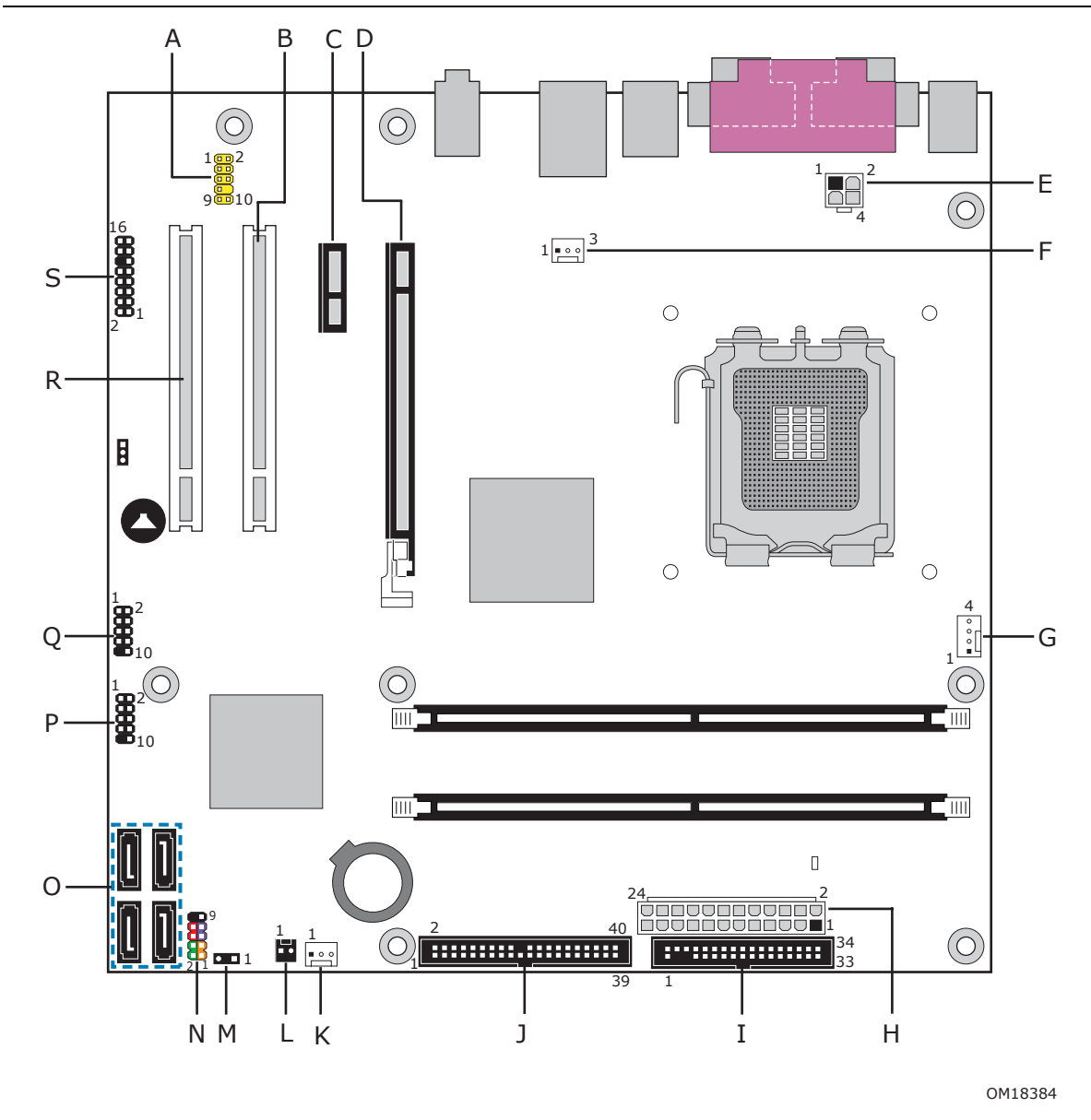
**Figure 13. Back Panel Connectors**

**NOTE**

*The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.*

## 2.7.2 Component-side Connectors and Headers

Figure 14 shows the locations of the component-side connectors and headers.



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**Figure 14. Component-side Connectors and Headers**

Table 15 lists the component-side connectors and headers identified in Figure 14.

**Table 15. Component-side Connectors and Headers Shown in Figure 14**

Item/callout from Figure 14	Description
A	Front panel audio header
B	PCI Conventional bus add-in card connector 1
C	PCI Express x1 add-in card connector
D	PCI Express x16 add-in card connector
E	Processor core power connector
F	Rear chassis fan header
G	Processor fan header
H	Main power connector
I	Diskette drive connector
J	Parallel ATA IDE connector
K	Front chassis fan header
L	Chassis intrusion header
M	Auxiliary front panel power LED header
N	Front panel header
O	Serial ATA connectors [4]
P	Front panel USB header
Q	Front panel USB header
R	PCI Conventional bus add-in card connector 2
S	High Definition Audio Link header

**Table 16. Front Panel Audio Header**

Pin	Signal Name	Pin	Signal Name
1	[Port 1] Left channel	2	Ground
3	[Port 1] Right channel	4	PRESENCE# (Dongle present)
5	[Port 2] Right channel	6	[Port 1] SENSE_RETURN
7	SENSE_SEND (Jack detection)	8	Key (no pin)
9	[Port 2] Left channel	10	[Port 2] SENSE_RETURN

**Table 17. Front and Rear Chassis Fan Headers**

Pin	Signal Name
1	Control
2	+12 V
3	Tach

**Table 18. Processor Fan Header**

Pin	Signal Name
1	Ground
2	+12 V
3	FAN_TACH
4	FAN_CONTROL

**Table 19. Chassis Intrusion Header**

Pin	Signal Name
1	Intruder
2	Ground

**Table 20. Serial ATA Connectors**

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

**Table 21. High Definition Audio Link Header**

Pin	Signal Name	Pin	Signal Name
1	BCLK	2	Ground
3	RST	4	3.3 V/1.5 V I/O
5	SYNC	6	Ground
7	SDO	8	3.3V_CORE
9	SDI	10	+12 V
11	No connect	12	Key (no pin)
13	No connect	14	3.3 V/1.5V STBY
15	No connect	16	Ground

### 2.7.2.1 Add-in Card Connectors

The board has the following add-in card connectors:

- PCI Express x16: one connector supporting simultaneous transfer speeds up to 4 GBytes/sec of peak bandwidth per direction and up to 8 GBytes/sec concurrent bandwidth
- PCI Express x1: one PCI Express x1 connector. The x1 interface supports simultaneous transfer speeds up to 250 Mbytes/sec of peak bandwidth per direction and up to 500 MBytes/sec concurrent bandwidth
- PCI Conventional (rev 2.3 compliant) bus: two PCI Conventional bus add-in card connectors. The SMBus is routed to PCI Conventional bus connector 2 only. PCI Conventional bus add-in cards with SMBus support can access sensor data and other information residing on the board.

Note the following considerations for the PCI Conventional bus connectors:

- All of the PCI Conventional bus connectors are bus master capable.
- SMBus signals are routed to PCI Conventional bus connector 2. This enables PCI Conventional bus add-in boards with SMBus support to access sensor data on the board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40.
  - The SMBus data line is connected to pin A41.

### 2.7.2.2 Power Supply Connectors

The board has the following power supply connectors:

- **Main power** – a 2 x 12 connector. This connector is compatible with 2 x 10 connectors previously used on Intel Desktop boards. The board supports the use of ATX12V power supplies with either 2 x 10 or 2 x 12 main power cables. When using a power supply with a 2 x 10 main power cable, attach that cable on the rightmost pins of the main power connector, leaving pins 11, 12, 23, and 24 unconnected.
- **Processor core power** – a 2 x 2 connector. This connector provides power directly to the processor voltage regulator and must always be used. Failure to do so will prevent the board from booting.

**Table 22. Processor Core Power Connector**

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Ground
3	+12 V	4	+12 V

**Table 23. Main Power Connector**

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	13	+3.3 V
2	+3.3 V	14	-12 V
3	Ground	15	Ground
4	+5 V	16	PS-ON# (power supply remote on/off)
5	Ground	17	Ground
6	+5 V	18	Ground
7	Ground	19	Ground
8	PWRGD (Power Good)	20	No connect
9	+5 V (Standby)	21	+5 V
10	+12 V	22	+5 V
11	+12 V (Note)	23	+5 V (Note)
12	2 x 12 connector detect (Note)	24	Ground (Note)

Note: When using a 2 x 10 power supply cable, this pin will be unconnected.

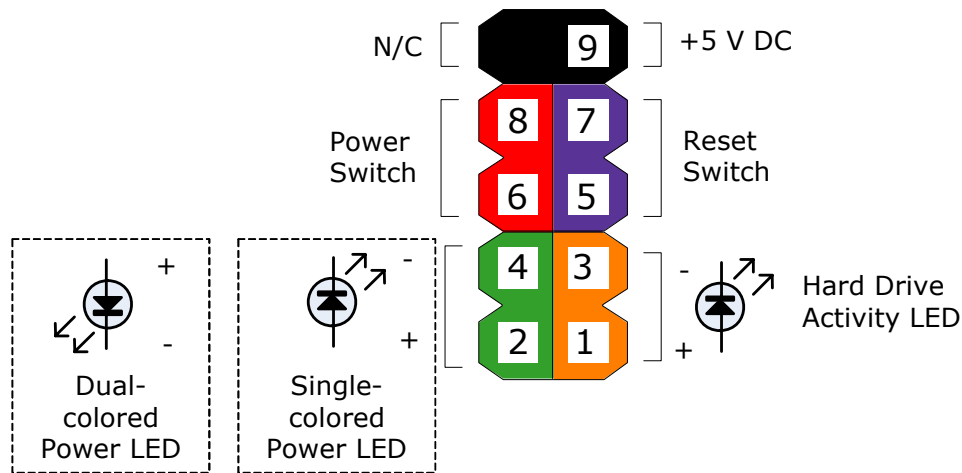


### 2.7.2.3 Front Panel Header

This section describes the functions of the front panel header. Table 24 lists the signal names of the front panel header. Figure 15 is a connection diagram for the front panel header.

**Table 24. Front Panel Header**

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
<b>Hard Drive Activity LED</b>				<b>Power LED</b>			
1	HD_PWR	Out	Hard disk LED pull-up to +5 V	2	HDR_BLNK_GRN	Out	Front panel green LED
3	HDA#	Out	Hard disk active LED	4	HDR_BLNK_YEL	Out	Front panel yellow LED
<b>Reset Switch</b>				<b>On/Off Switch</b>			
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
<b>Power</b>				<b>Not Connected</b>			
9	+5 V		Power	10	N/C		Not connected



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**Figure 15. Connection Diagram for Front Panel Header**

#### 2.7.2.3.1 Hard Drive Activity LED Header

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires one of the following:

- A Serial ATA hard drive connected to an onboard Serial ATA connector
- A Parallel ATA IDE hard drive connected to an onboard Parallel ATA IDE connector

**2.7.2.3.2 Reset Switch Header**

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

**2.7.2.3.3 Power/Sleep LED Header**

Pins 2 and 4 can be connected to a one- or two-color LED. Table 25 shows the possible states for a one-color LED. Table 26 shows the possible states for a two-color LED.

**Table 25. States for a One-Color Power LED**

LED State	Description
Off	Power off/sleeping
Steady Green	Running

**Table 26. States for a Two-Color Power LED**

LED State	Description
Off	Power off
Steady Green	Running
Steady Yellow	Sleeping

 **NOTE**

*The colors listed in Table 25 and Table 26 are suggested colors only. Actual LED colors are product- or customer-specific.*

**2.7.2.3.4 Power Switch Header**

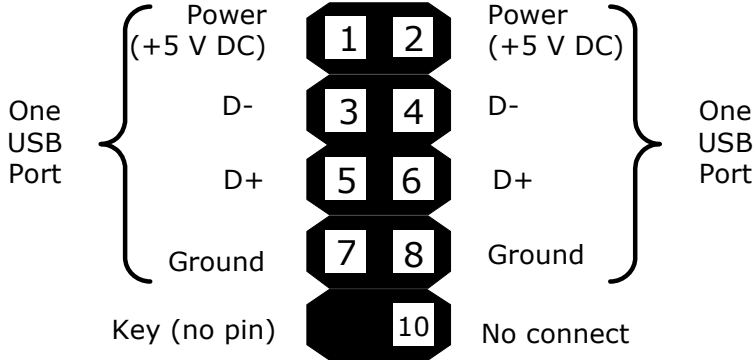
Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW\_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

### 2.7.2.4 Front Panel USB Headers

Figure 16 is a connection diagram for the front panel USB headers.

**⚠ INTEGRATOR'S NOTES**

- The +5 V DC power on the USB headers is fused.
- Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.



OM18317

**Figure 16. Connection Diagram for Front Panel USB Headers**

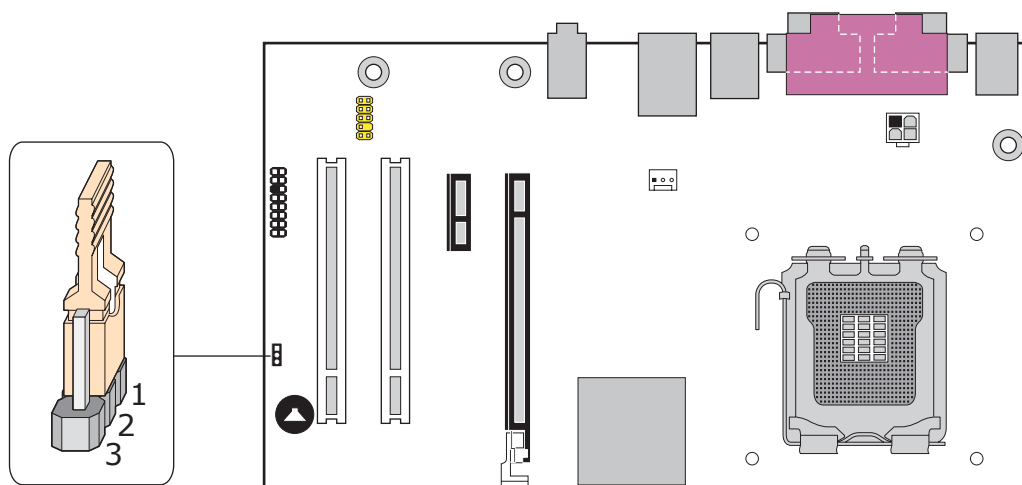
## 2.8 Jumper Block



### CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

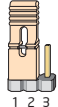
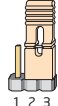

Figure 17 shows the location of the jumper block. The jumper determines the BIOS Setup program's mode. Table 27 lists the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configure mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.



OM18385

**Figure 17. Location of the Jumper Block**

**Table 27. BIOS Setup Configuration Jumper Settings**

Function/Mode	Jumper Setting	Configuration
Normal	1-2 	The BIOS uses current configuration information and passwords for booting.
Configure	2-3 	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None 	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

## 2.9 Mechanical Considerations

### 2.9.1 Form Factor

The board is designed to fit into an ATX- or microATX-form-factor chassis. Figure 18 illustrates the mechanical form factor for the board. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 9.60 inches [243.84 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.

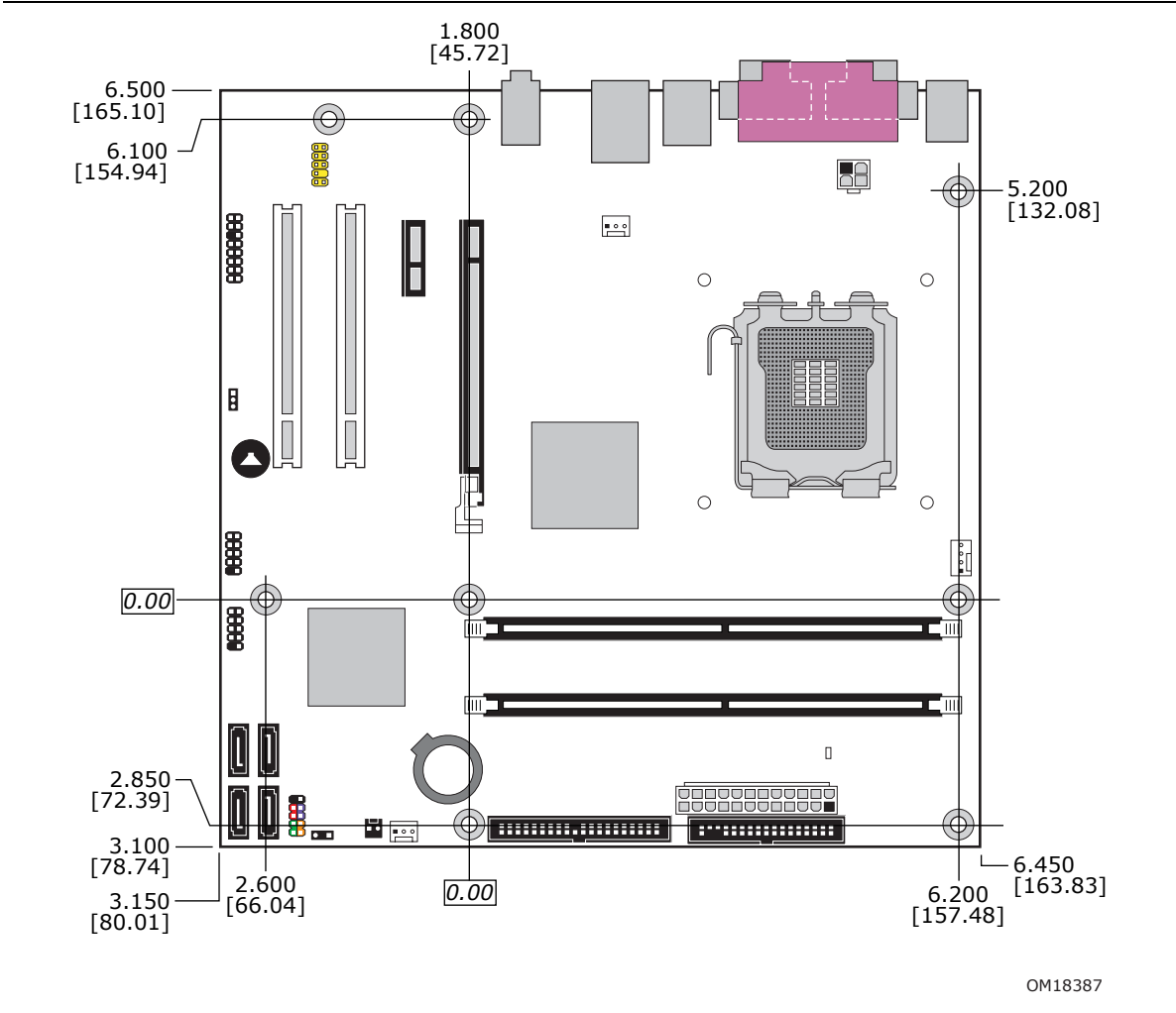


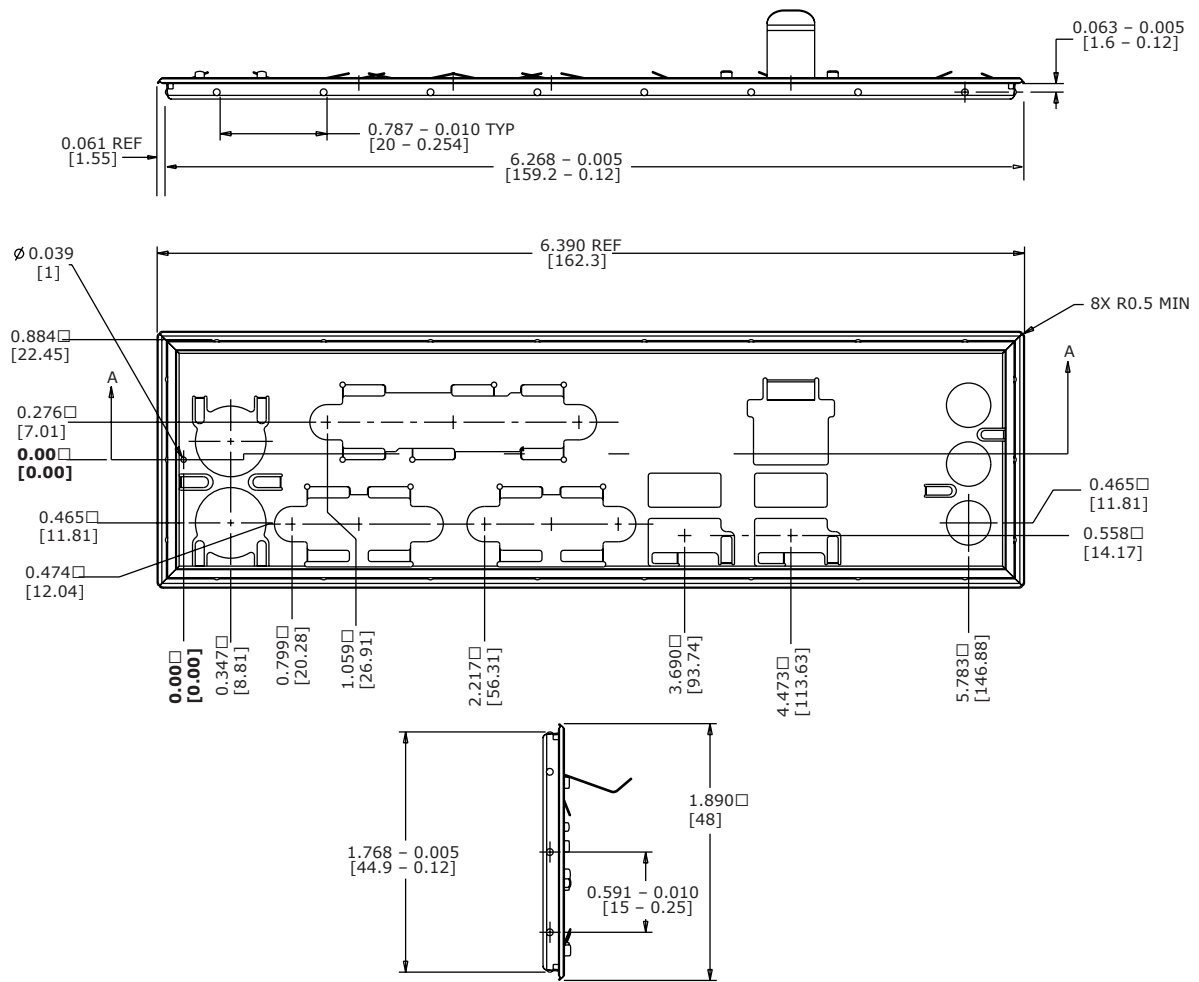
Figure 18. Board Dimensions

## 2.9.2 I/O Shield

The back panel I/O shield for the board must meet specific dimension and material requirements. Systems based on this board need the back panel I/O shield to pass certification testing. Figure 19 shows the I/O shield. The figure indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification.

**NOTE**

*The I/O shield drawing is for reference only.*



OM18411

**Figure 19. I/O Shield Dimensions**

## 2.10 Electrical Considerations

### 2.10.1 DC Loading

Table 28 lists the DC loading characteristics of the board. This data is based on a DC analysis of all active components within the board that impact its power delivery subsystems. The analysis does not include PCI add-in cards. Minimum values assume a light load placed on the board that is similar to an environment with no applications running and no USB current draw. Maximum values assume a load placed on the board that is similar to a heavy gaming environment with a 500 mA current draw per USB port. These calculations are not based on specific processor values or memory configurations but are based on the minimum and maximum current draw possible from the board’s power delivery subsystems to the processor, memory, and USB ports.

Use the datasheets for add-in cards, such as PCI, to determine the overall system power requirements. The selection of a power supply at the system level is dependent on the system’s usage model and not necessarily tied to a particular processor speed.

**Table 28. DC Loading Characteristics**

Mode	DC Power	DC Current at:					
		-12 V	+12 V1	+12 V2 (CPU)	+5 V	+3.3 v	+5 VSB
Minimum loading	43.13 W	0.00	0.40	1.79	1.80	2.00	0.25 [S0] 0.25 [S3]
Maximum loading	532.98 W	0.30	11.50	16.77	23.97	19.52	1.18 [S0] 2.00 [S3]

### 2.10.2 Fan Header Current Capability



#### CAUTION

*The processor fan must be connected to the processor fan header, not to a chassis fan header. Connecting the processor fan to a chassis fan header may result in onboard component damage that will halt fan operation.*

Table 29 lists the current capability of the fan headers.

**Table 29. Fan Header Current Capability**

Fan Header	Maximum Available Current
Processor fan	2.0 A
Front chassis fan	1.5 A
Rear chassis fan	1.5 A

### 2.10.3 Add-in Board Considerations

The board is designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards for a fully loaded board (all three expansion slots and the PCI Express x16 connector filled) must not exceed 8 A.

### 2.10.4 Power Supply Considerations



#### **CAUTION**

*The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.*

System integrators should refer to the power usage values listed in Table 28 when selecting a power supply for use with the board.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the indicated parameters of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails
- The current capability of the +5 VSB line
- All timing parameters
- All voltage tolerances



## 2.11 Thermal Considerations



### CAUTION

*A chassis with a maximum internal ambient temperature of 38 °C at the processor fan inlet is a requirement. Use a processor heatsink that provides omni-directional airflow to maintain required airflow across the processor voltage regulator area.*



### CAUTION

*Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board. For a list of chassis that have been tested with Intel desktop boards please refer to the following website:*

<http://developer.intel.com/design/motherbd/cooling.htm>

*All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.*



### CAUTION

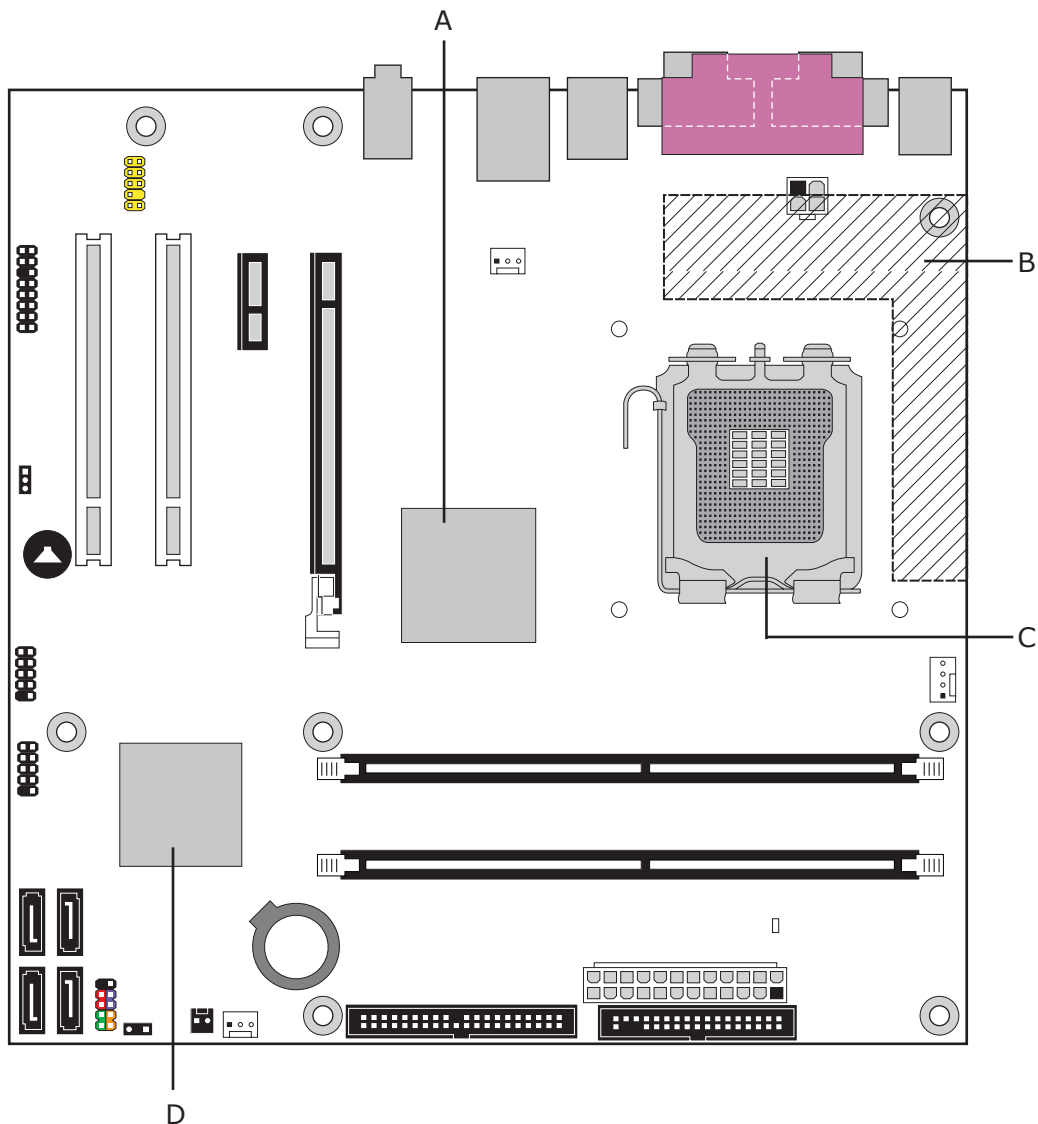
*Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.13.*



### CAUTION

*Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (shown in Figure 20) can reach a temperature of up to 85 °C in an open chassis.*

Figure 20 shows the locations of the localized high temperature zones.



OM18386

Item	Description
A	Intel 82946GZ GMCH
B	Processor voltage regulator area
C	Processor
D	Intel 82801GB ICH7

**Figure 20. Localized High Temperature Zones**

Table 30 provides maximum case temperatures for the board components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

**Table 30. Thermal Considerations for Components**

Component	Maximum Case Temperature
Processor	For processor case temperature, see processor datasheets and processor specification updates
Intel 82946GZ MCH	99 °C (under bias)
Intel 82801GB ICH7	115 °C (under bias)
<b>For information about</b>	<b>Refer to</b>
Processor datasheets and specification updates	Section 1.2, page 15

## 2.12 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 55 °C. The Desktop Board D946GZIS MTBF is 132,431.56 hours.

## 2.13 Environmental

Table 31 lists the environmental specifications for the board.

**Table 31. Desktop Board D946GZIS Environmental Specifications**

Parameter	Specification		
<b>Temperature</b>			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
<b>Shock</b>			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second <sup>2</sup>		
Packaged	Half sine 2 millisecond		
	Product weight (pounds)	Free fall (inches)	Velocity change (inches/sec <sup>2</sup> )
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
<b>Vibration</b>			
Unpackaged	5 Hz to 20 Hz: 0.01 g <sup>2</sup> Hz sloping up to 0.02 g <sup>2</sup> Hz		
	20 Hz to 500 Hz: 0.02 g <sup>2</sup> Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g <sup>2</sup> Hz (flat)		
	40 Hz to 500 Hz: 0.015 g <sup>2</sup> Hz sloping down to 0.00015 g <sup>2</sup> Hz		

## 2.14 Regulatory Compliance

This section contains the following regulatory compliance information for Desktop Board D946GZIS:

- Safety regulations
- European Union Declaration of Conformity statement
- Product Ecology statements
- Electromagnetic Compatibility (EMC) regulations
- Product certification markings

### 2.14.1 Safety Regulations

Desktop Board D946GZIS complies with the safety regulations stated in Table 32 when correctly installed in a compatible host system.

**Table 32. Safety Regulations**

Regulation	Title
UL 60950-1:2003/ CSA C22.2 No. 60950-1-03	Information Technology Equipment – Safety - Part 1: General Requirements (USA and Canada)
EN 60950-1:2002	Information Technology Equipment – Safety - Part 1: General Requirements (European Union)
IEC 60950-1:2001, First Edition	Information Technology Equipment – Safety - Part 1: General Requirements (International)

### 2.14.2 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product Intel® Desktop Board D946GZIS is in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 89/336/EEC (EMC Directive) and Council Directive 73/23/EEC (Safety/Low Voltage Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.



This product follows the provisions of the European Directives 89/336/EEC and 73/23/EEC.

**Čeština** Tento výrobek odpovídá požadavkům evropských směrnic 89/336/EEC a 73/23/EEC.

**Dansk** Dette produkt er i overensstemmelse med det europæiske direktiv 89/336/EEC & 73/23/EEC.

**Dutch** Dit product is in navolging van de bepalingen van Europees Directief 89/336/EEC & 73/23/EEC.

**Eesti** Antud toode vastab Euroopa direktiivides 89/336/EEC ja 73/23/EEC kehtestatud nõuetele.

**Suomi** Tämä tuote noudattaa EU-direktiivin 89/336/EEC & 73/23/EEC määräyksiä.

**Français** Ce produit est conforme aux exigences de la Directive Européenne 89/336/EEC & 73/23/EEC.

**Deutsch** Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 89/336/EEC & 73/23/EEC.

**Ελληνικά** Το παρόν προϊόν ακολουθεί τις διατάξεις των Ευρωπαϊκών Οδηγιών 89/336/ΕΟΚ και 73/23/ΕΟΚ.

**Magyar** E termék megfelel a 89/336/EEC és 73/23/EEC Európai Irányelv előírásainak.

**Icelandic** Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 89/336/ EEC & 73/23/EEC.

**Italiano** Questo prodotto è conforme alla Direttiva Europea 89/336/EEC & 73/23/EEC.

**Latviešu** Šis produkts atbilst Eiropas Direktīvu 89/336/EEC un 73/23/EEC noteikumiem.

**Lietuvių** Šis produktas atitinka Europos direktyvų 89/336/EEC ir 73/23/EEC nuostatas.

**Malti** Dan il-prodott hu konformi mal-provvedimenti tad-Direttivi Ewropej 89/336/EEC u 73/23/EEC.

**Norsk** Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 89/336/ EEC & 73/23/EEC.

**Polski** Niniejszy produkt jest zgodny z postanowieniami Dyrektyw Unii Europejskiej 89/336/EWG i 73/23/EWG.

**Portuguese** Este produto cumpre com as normas da Diretiva Europeia 89/336/EEC & 73/23/EEC.

**Español** Este producto cumple con las normas del Directivo Europeo 89/336/EEC & 73/23/EEC.

**Slovensky** Tento produkt je v súlade s ustanoveniami európskych direktív 89/336/EEC a 73/23/EEC.

**Slovenščina** Izdelek je skladen z določbami evropskih direktiv 89/336/EGS in 73/23/EGS.

**Svenska** Denna produkt har tillverkats i enlighet med EG-direktiv 89/336/EEC & 73/23/EEC.

**Türkçe** Bu ürün, Avrupa Birliği'nin 89/336/EEC ve 73/23/EEC yönergelerine uyar.

### 2.14.3 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

#### 2.14.3.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

#### 2.14.3.2 Recycling Considerations

As part of its commitment to environmental responsibility, Intel has implemented the Intel Product Recycling Program to allow retail consumers of Intel's branded products to return used products to select locations for proper recycling.

Please consult the

[http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm) for the details of this program, including the scope of covered products, available locations, shipping instructions, terms and conditions, etc.

#### **中文**

作为其对环境责任之承诺的部分，英特尔已实施 Intel Product Recycling Program（英特尔产品回收计划），以允许英特尔品牌产品的零售消费者将使用过的产品退还至指定地点作恰当的重复使用处理。

请参考[http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm)了解此计划的详情，包括涉及产品之范围、回收地点、运送指导、条款和条件等。

#### **Deutsch**

Als Teil von Intels Engagement für den Umweltschutz hat das Unternehmen das Intel Produkt-Recyclingprogramm implementiert, das Einzelhandelskunden von Intel Markenprodukten ermöglicht, gebrauchte Produkte an ausgewählte Standorte für ordnungsgemäßes Recycling zurückzugeben.

Details zu diesem Programm, einschließlich der darin eingeschlossenen Produkte, verfügbaren Standorte, Versandanweisungen, Bedingungen usw., finden Sie auf der [http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm)

#### **Español**

Como parte de su compromiso de responsabilidad medioambiental, Intel ha implantado el programa de reciclaje de productos Intel, que permite que los consumidores al detalle de los productos Intel devuelvan los productos usados en los lugares seleccionados para su correspondiente reciclado.

Consulte la

[http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm) para ver los detalles del programa, que incluye los productos que abarca, los lugares disponibles, instrucciones de envío, términos y condiciones, etc.

**Français**

Dans le cadre de son engagement pour la protection de l'environnement, Intel a mis en œuvre le programme Intel Product Recycling Program (Programme de recyclage des produits Intel) pour permettre aux consommateurs de produits Intel de recycler les produits usés en les retournant à des adresses spécifiées.

Visitez la page Web

[http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm) pour en savoir plus sur ce programme, à savoir les produits concernés, les adresses disponibles, les instructions d'expédition, les conditions générales, etc.

**日本語**

インテルでは、環境保護活動の一環として、使い終えたインテルブランド製品を指定の場所へ返送していただき、リサイクルを適切に行えるよう、インテル製品リサイクルプログラムを発足させました。

対象製品、返送先、返送方法、ご利用規約など、このプログラムの詳細情報は、[http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm) (英語)をご覧ください。

**Malay**

Sebagai sebahagian daripada komitmennya terhadap tanggungjawab persekitaran, Intel telah melaksanakan Program Kitar Semula Produk untuk membenarkan pengguna-pengguna runcit produk jenama Intel memulangkan produk terguna ke lokasi-lokasi terpilih untuk dikitar semula dengan betul.

Sila rujuk

[http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm) untuk mendapatkan butir-butir program ini, termasuklah skop produk yang dirangkumi, lokasi-lokasi tersedia, arahan penghantaran, terma & syarat, dsb.

**Portuguese**

Como parte deste compromisso com o respeito ao ambiente, a Intel implementou o Programa de Reciclagem de Produtos para que os consumidores finais possam enviar produtos Intel usados para locais selecionados, onde esses produtos são reciclados de maneira adequada.

Consulte o site

[http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm) (em Inglês) para obter os detalhes sobre este programa, inclusive o escopo dos produtos cobertos, os locais disponíveis, as instruções de envio, os termos e condições, etc.

**Russian**

В качестве части своих обязательств к окружающей среде, в Intel создана программа утилизации продукции Intel (Product Recycling Program) для предоставления конечным пользователям марок продукции Intel возможности возврата используемой продукции в специализированные пункты для должной утилизации.

Пожалуйста, обратитесь на веб-сайт

[http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm) за информацией об этой программе, принимаемых продуктах, местах приема, инструкциях об отправке, положениях и условиях и т.д.

**Türkçe**

Intel, çevre sorumluluğuna bağlılığının bir parçası olarak, perakende tüketicilerin Intel markalı kullanılmış ürünlerini belirlenmiş merkezlere iade edip uygun şekilde geri dönüştürmesini amaçlayan Intel Ürünleri Geri Dönüşüm Programı'nı uygulamaya koymuştur.

Bu programın ürün kapsamı, ürün iade merkezleri, nakliye talimatları, kayıtlar ve şartlar v.s dahil bütün ayrıntılarını öğrenmek için lütfen


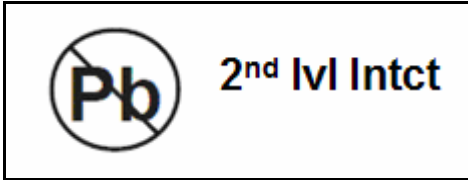

[http://www.intel.com/intel/other/ehs/product\\_ecology/Recycling\\_Program.htm](http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm)

Web sayfasına gidin.

**2.14.3.3 Lead Free Desktop Board**

This desktop board is lead free although certain discrete components used on the board contain a small amount of lead which is necessary for component performance and/or reliability. This desktop board is referred to as "Lead-free second level interconnect." The board substrate and the solder connections from the board to the components (second-level connections) are all lead free. Table 33 shows the various forms of the "Lead-Free 2<sup>nd</sup> Level Interconnect" mark as it appears on the board and accompanying collateral.

**Table 33. Lead-Free Board Markings**

Description	Mark
<p><b>Lead-Free 2<sup>nd</sup> Level Interconnect:</b> This symbol is used to identify electrical and electronic assemblies and components in which the lead (Pb) concentration level in the desktop board substrate and the solder connections from the board to the components (second-level interconnect) is not greater than 0.1% by weight (1000 ppm).</p>	<div style="text-align: center;">  <p>or</p>  <p>or</p>  </div>



## 2.14.4 EMC Regulations

Desktop Board D946GZIS complies with the EMC regulations stated in Table 34 when correctly installed in a compatible host system.

**Table 34. EMC Regulations**

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radio Frequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022: 1998 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS CISPR 22 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 3rd Edition, (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurement. (International)
VCCI (Class B)	Voluntary Control for Interference by Information Technology Equipment. (Japan)

Japanese Kanji statement translation: this is a Class B product based on the standard of the Voluntary Control Council for Interference from Information Technology Equipment (VCCI). If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

この装置は、情報処理装置等電波障害自主規制協議会（VCCI）の基準に基づくクラスB情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。  
取扱説明書に従って正しい取り扱いをして下さい。








Korean Class B statement translation: this is household equipment that is certified to comply with EMC requirements. You may use this equipment in residential environments and other non-residential environments.

이 기기는 가정용으로 전자파적합등록을 한 기기로서  
주거지역에서는 물론 모든 지역에서 사용할 수 있습니다.

### 2.14.5 Product Certification Markings (Board Level)

Desktop Board D946GZIS has the product certification markings shown in Table 35:

**Table 35. Product Certification Markings**

Description	Mark
UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel desktop boards: E210882.	
FCC Declaration of Conformity logo mark for Class B equipment. Includes Intel name and D946GZIS model designation.	
CE mark. Declaring compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC).	
Australian Communications Authority (ACA) C-tick mark. Includes adjacent Intel supplier code number, N-232.	
Japan VCCI (Voluntary Control Council for Interference) mark.	
S. Korea MIC (Ministry of Information and Communication) mark. Includes adjacent MIC certification number: CPU-D946GZIS  For information about MIC certification, go to <a href="http://support.intel.com/support/motherboards/desktop/">http://support.intel.com/support/motherboards/desktop/</a>	
Taiwan BSMI (Bureau of Standards, Metrology and Inspections) mark. Includes adjacent Intel company number, D33025.	
Printed wiring board manufacturer's recognition mark. Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side).	V-0

## 3 Overview of BIOS Features

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### 3.1 Introduction

The board uses an Intel BIOS that is stored in the Serial Peripheral Interface Flash Memory (SPI Flash) and can be updated using a disk-based program. The SPI Flash contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as TS94610J.86A.

When the BIOS Setup configuration jumper is set to configure mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
-------------	------	----------	----------	-------	------	------

#### NOTE

*The maintenance menu is displayed only when the board is in configure mode. Section 2.8 on page 60 shows how to put the board in configure mode.*

Table 36 lists the BIOS Setup program menu features.

**Table 36. BIOS Setup Program Menu Bar**

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and displays processor information	Displays processor and memory configuration	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features and power supply controls	Selects boot options	Saves or discards changes to Setup program options

Table 37 lists the function keys available for menu screens.

**Table 37. BIOS Setup Program Function Keys**

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

## 3.2 BIOS Flash Memory Organization

The Serial Peripheral Interface Flash Memory (SPI Flash) includes an 4 Mbit (512 KB) flash memory device

## 3.3 Resource Configuration

### 3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

### 3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the PCI IDE connector with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

#### **NOTE**

*Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.*

## 3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT\*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

## 3.5 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

## 3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

### NOTE

*Review the instructions distributed with the upgrade utility before attempting a BIOS update.*

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<b>For information about</b>	<b>Refer to</b>
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The Intel World Wide Web site	Section 1.2, page 15
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### 3.6.1 Language Support

The BIOS Setup program and help messages are supported in US English. Additional languages are available in the Integrator's Toolkit utility. Check the Intel website for details.

### 3.6.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. The Integrator's Toolkit that is available from Intel can be used to create a custom splash screen.

#### NOTE

*If you add a custom splash screen, it will share space with the Intel branded logo.*

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 15

## 3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

### 3.7.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

### 3.7.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

### 3.7.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

### 3.7.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program's Boot Device Priority Submenu). Table 38 lists the boot device menu options.

**Table 38. Boot Device Menu Options**

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without saving changes

## 3.8 Adjusting Boot Speed

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Optimized BIOS boot parameters

### 3.8.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as "power-up to data ready" less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.



### 3.8.2 BIOS Boot Optimizations

Use of the following BIOS Setup program settings reduces the POST execution time.

- In the Boot Menu, set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

#### NOTE

*It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.*

*This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from three to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the Drive Configuration Submenu of the BIOS Setup program).*

## 3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.

Table 39 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

**Table 39. Supervisor and User Password Functions**

<b>Password Set</b>	<b>Supervisor Mode</b>	<b>User Mode</b>	<b>Setup Options</b>	<b>Password to Enter Setup</b>	<b>Password During Boot</b>
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

# 4 Error Messages and Beep Codes

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### 4.1 Speaker

The board-mounted speaker provides audible error code (beep code) information during POST.

<b>For information about</b>	<b>Refer to</b>
The location of the onboard speaker	Figure 1, page 12

### 4.2 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 40).

**Table 40. Beep Codes**

<b>Type</b>	<b>Pattern</b>	<b>Frequency</b>
Memory error	Three long beeps	1280 Hz
Thermal warning	Four alternating beeps: High tone, low tone, high tone, low tone	High tone: 2000 Hz Low tone: 1600 Hz

### 4.3 BIOS Error Messages

Table 41 lists the error messages and provides a brief description of each.

**Table 41. BIOS Error Messages**

<b>Error Message</b>	<b>Explanation</b>
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.

## 4.4 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

### ⇒ NOTE

*The POST card must be installed in PCI bus connector 1.*

The following tables provide information about the POST codes generated by the BIOS:

- Table 42 lists the Port 80h POST code ranges
- Table 43 lists the Port 80h POST codes themselves
- Table 44 lists the Port 80h POST sequence

### ⇒ NOTE

*In the tables listed above, all POST codes and range values are listed in hexadecimal.*

**Table 42. Port 80h POST Code Ranges**

Range	Category/Subsystem
00 – 0F	Debug codes: Can be used by any PEIM/driver for debug.
10 – 1F	Host Processors: 1F is an unrecoverable CPU error.
20 – 2F	Memory/Chipset: 2F is no memory detected or no useful memory detected.
30 – 3F	Recovery: 3F indicated recovery failure.
40 – 4F	Reserved for future use.
50 – 5F	I/O Busses: PCI, USB, ISA, ATA, etc. 5F is an unrecoverable error. Start with PCI.
60 – 6F	Reserved for future use (for new busses).
70 – 7F	Output Devices: All output consoles. 7F is an unrecoverable error.
80 – 8F	Reserved for future use (new output console codes).
90 – 9F	Input devices: Keyboard/Mouse. 9F is an unrecoverable error.
A0 – AF	Reserved for future use (new input console codes).
B0 – BF	Boot Devices: Includes fixed media and removable media. BF is an unrecoverable error.
C0 – CF	Reserved for future use.
D0 – DF	Boot device selection.
E0 – FF	F0 – FF: FF processor exception. E0 – EE: Miscellaneous codes. See Table 43. EF boot/S3: resume failure.

**Table 43. Port 80h POST Codes**

<b>POST Code</b>	<b>Description of POST Operation</b>
<b>Host Processor</b>	
10	Power-on initialization of the host processor (Boot Strap Processor)
11	Host processor Cache initialization (including APs)
12	Starting Application processor initialization
13	SMM initialization
<b>Chipset</b>	
21	Initializing a chipset component
<b>Memory</b>	
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
24	Programming timing parameters in the memory controller and the DIMMs
25	Configuring memory
26	Optimizing memory settings
27	Initializing memory, such as ECC init
28	Testing memory
<b>PCI Bus</b>	
50	Enumerating PCI busses
51	Allocating resources to PCI bus
52	Hot Plug PCI controller initialization
53 – 57	Reserved for PCI Bus
<b>USB</b>	
58	Resetting USB bus
59	Reserved for USB
<b>ATA/ATAPI/SATA</b>	
5A	Resetting PATA/SATA bus and all devices
5B	Reserved for ATA
<b>SMBus</b>	
5C	Resetting SMBUS
5D	Reserved for SMBUS
<b>Local Console</b>	
70	Resetting the VGA controller
71	Disabling the VGA controller
72	Enabling the VGA controller
<b>Remote Console</b>	
78	Resetting the console controller
79	Disabling the console controller
7A	Enabling the console controller

continued

**Table 43. Port 80h POST Codes** (continued)

<b>POST Code</b>	<b>Description of POST Operation</b>
<b>Keyboard (PS2 or USB)</b>	
90	Resetting keyboard
91	Disabling keyboard
92	Detecting presence of keyboard
93	Enabling the keyboard
94	Clearing keyboard input buffer
95	Instructing keyboard controller to run Self Test (PS2 only)
<b>Mouse (PS2 or USB)</b>	
98	Resetting mouse
99	Disabling mouse
9A	Detecting presence of mouse
9B	Enabling mouse
<b>Fixed Media</b>	
B0	Resetting fixed media
B1	Disabling fixed media
B2	Detecting presence of a fixed media (IDE hard drive detection etc.)
B3	Enabling/configuring a fixed media
<b>Removable Media</b>	
B8	Resetting removable media
B9	Disabling removable media
BA	Detecting presence of a removable media (IDE, CD-ROM detection, etc.)
BC	Enabling/configuring a removable media
<b>BDS</b>	
Dy	Trying boot selection y (y=0 to 15)
<b>PEI Core</b>	
E0	Started dispatching PEIMs (emitted on first report of EFI_SW_PC_INIT_BEGIN EFI_SW_PEI_PC_HANDOFF_TO_NEXT)
E2	Permanent memory found
E1, E3	Reserved for PEI/PEIMs
<b>DXE Core</b>	
E4	Entered DXE phase
E5	Started dispatching drivers
E6	Started connecting drivers

continued

**Table 43. Port 80h POST Codes** (continued)

<b>POST Code</b>	<b>Description of POST Operation</b>
<b>DXE Drivers</b>	
E7	Waiting for user input
E8	Checking password
E9	Entering BIOS setup
EA	TBD – Flash Update
EB	Calling Legacy Option ROMs
EE	TBD – Calling INT 19. One beep unless silent boot is enabled
EF	TBD – Unrecoverable Boot failure/S3 resume failure
<b>Runtime Phase/EFI OS Boot</b>	
F4	Entering Sleep state
F5	Exiting Sleep state
F8	EFI boot service ExitBootServices ( ) has been called
F9	EFI runtime service SetVirtualAddressMap ( ) has been called
FA	EFI runtime service ResetSystem ( ) has been called
<b>PEIMs/Recovery</b>	
30	Crisis Recovery has initiated per User request
31	Crisis Recovery has initiated by software (corrupt flash)
34	Loading recovery capsule
35	Handing off control to the recovery capsule
3F	Unable to recover

**Table 44. Typical Port 80h POST Sequence**

<b>POST Code</b>	<b>Description</b>
21	Initializing a chipset component
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
25	Configuring memory
28	Testing memory
34	Loading recovery capsule
E4	Entered DXE phase
12	Starting Application processor initialization
13	SMM initialization
50	Enumerating PCI busses
51	Allocating resourced to PCI bus
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
95	Keyboard Self Test
EB	Calling Video BIOS
58	Resetting USB bus
5A	Resetting PATA/SATA bus and all devices
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
5A	Resetting PATA/SATA bus and all devices
28	Testing memory
90	Resetting keyboard
94	Clearing keyboard input buffer
E7	Waiting for user input
01	INT 19
00	Ready to boot